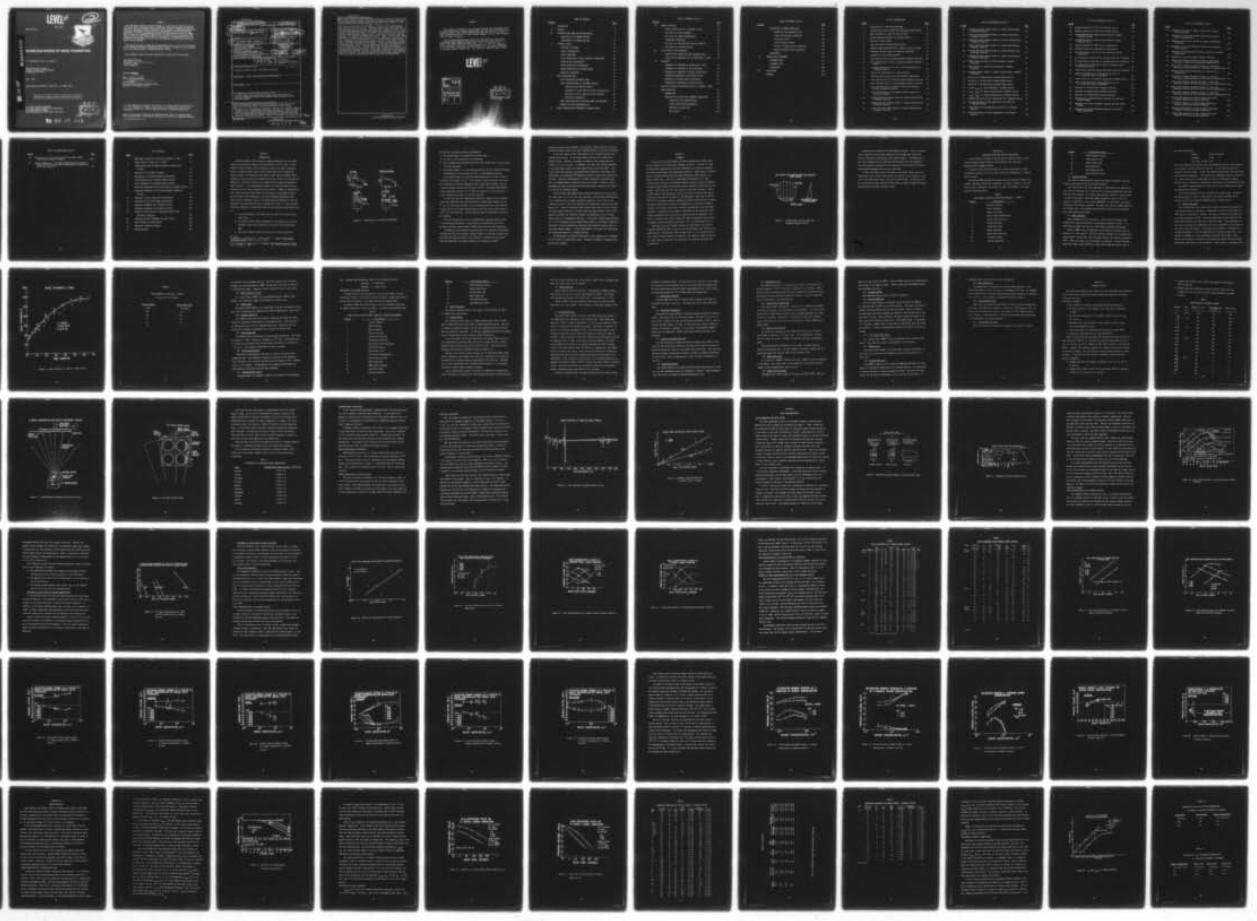
AD-A068 493 GENERAL ELECTRIC CORPORATE RESEARCH AND DEVELOPMENT --ETC F/G 9/1
INTERFACE DOPING OF MNOS TRANSISTORS.(U)
JUN 78 C A NEUGEBAUER, M M BARNICLE F33615-76-C-1035
UNCLASSIFIED SRD-78-097 AFAL-TR-78-87 NL

1 OF 3
AD A068493



LEVEL III

2

SC

AD A067857

AFAL-TR-78-87

AD A068493

DDC FILE COPY

INTERFACE DOPING OF MNOS TRANSISTORS

C. A. Neugebauer and M. M. Barnicle

General Electric Company
Corporate Research & Development
Schenectady, NY 12345

June 1978

FINAL REPORT FOR PERIOD 1 APRIL 1976 - 31 MARCH 1978

Approved for public release; distribution unlimited.

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
AIR FORCE SYSTEMS COMMAND
WRIGHT-PATTERSON AIR FORCE BASE, OHIO 45433

DDC
RECEIVED
MAY 9 1979
D

79 05 07 045

NOTICE

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

This report has been reviewed by the Information Office (OI) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

Dr. Millard G. Mier

MILLARD G. MIER
Project Engineer

FOR THE COMMANDER

D. C. Reynolds

D. C. REYNOLDS
Acting Chief, Electronic Research Branch
Electronic Technology Division

"If your address has changed, if you wish to be removed from our mailing list, or if the addressee is no longer employed by your organization please notify AFAL(DHR) *,W-PAFB, OH 45433 to help us maintain a current mailing list".*

Copies of this report should not be returned unless return is required by security considerations, contractual obligations, or notice on a specific document.

AIR FORCE/56780/23 April 1979 — 150

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: AFAL-TR-78-87	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): INTERFACE DOPING OF MNOS TRANSISTORS.	5. TYPE OF REPORT & PERIOD COVERED: Final Technical Report. 1 Apr 76 - 31 Mar 78
6. PERFORMING ORG. REPORT NUMBER: SRD-78-097	
7. AUTHOR(s): C. A. Neugebauer and M. M. Barnicle	8. CONTRACT OR GRANT NUMBER(s): F33615-76-C-1035
9. PERFORMING ORGANIZATION NAME AND ADDRESS: General Electric Company, Corporate Research and Development, Schenectady, NY 12345	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: Project 2305/R1/61
11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Avionics Laboratory (DHR), Air Force Wright Aeronautical Laboratories, Wright Patterson AFB, Ohio 45433	12. REPORT DATE: June 1978 13. NUMBER OF PAGES: 207
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

611 02F

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Interface Doping, MNOS, Semiconductor Memory, Write Characteristics, Retention, Endurance, Nitride, Fowler-Nordheim Tunneling, Memory Window, Radiation Hardness

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This Final Technical Report describes the progress for the entire period, 1 April 1976 to March 1978, of the Interface Doping of MNOS program.

The objective of this program is threefold: First to survey interface dopants suitable for use in MNOS nonvolatile storage transistors, to identify optimum dopant materials, concentrations, and deposition techniques, and to evaluate the write characteristics, retention, and endurance of interface doped MNOS devices by accelerated test methods. Second, to investigate the feasibility of

→over

DD FORM 1 JAN 73 1473

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

406617

fabricating n-channel interface doped MNOS transistors, both memory and stable gate and assess device yields. Third, to investigate their radiation hardness toward total dose ionizing radiation.

The principal conclusions are as follows: (1) The six most promising dopants are: Pt, W, Cr, Ni, Pd, Ir. (2) The stored charge is principally negative. A one-transistor cell is, therefore, compatible with n-channel circuitry. (3) Interface doped MNOS devices differ from undoped ones principally in their ability to eject stored negative charge. (4) Thinner oxide, thinner nitride, and high dopant concentration give a faster device. Write times as short as 2 nsec are possible. (5) Interface doped MNOS devices have higher retention than undoped MNOS devices of equivalent write speed. Even the retention of fast write (< 1 μs) devices can be very long (10^5 to 10^{17} s). (6) Thick oxide, thick nitride, and a low dopant concentration favor higher retention. (7) Retention is controlled by back-tunneling between 77^{o}K and 300^{o}C. (8) Write/erase cycling does not affect retention. (9) The effective endurance of interface doped MNOS devices is 10^3 write/erase cycles. (10) One cannot trade retention for endurance. (11) N-channel differ from p-channel devices only in that surface states are not generated with write/erase cycling. (12) Attempts to fabricate Al gate memory transistors and n-channel silicon gate stable gate transistors on the same chip were not successful. (13) Hardness toward total dose ionizing radiation is 10^5 rads (Si) for zero or negative bias, and 10^4 rads (Si) for positive bias.

FOREWORD

This report was prepared by the Corporate Research and Development Center of the General Electric Company, Schenectady, New York under USAF Contract No. F33615-76-C-1035. The work was administered under the direction of the Air Force Avionics Laboratory, Air Force Systems Command, with Mr. John Blasingame (DHR) as project scientist.

The research covered in this report was conducted from 1 April 1976 to 31 March 1978. AFAL-TR-77-111 covered research under this contract conducted from 1 April 1976 to 31 March 1977. Dr. C. A. Neugebauer and Ms M. M. Barnicle carried out the experimental work. Dr. C. A. Neugebauer was the principal investigator and the supervisor of the program as Manager of the Power Module & Hybrid Unit. This report was submitted June 30, 1978.

LEVEL II

ACCESSION for
NTIS White Section
DDC Buff Section
UNANNOUNCED
JUSTIFICATION
BY
DISTRIBUTION/AVAILABILITY CODES
Dist. AVAIL. and/or SPECIAL
A

A067857

DDC
RECEIVED
MAY 9 1979
D

TABLE OF CONTENTS

SECTION		PAGE
I	INTRODUCTION	1
II	APPROACH	5
III	INTERFACE-DOPED MNOS DEVICE FABRICATION	8
	FABRICATION OF P-CHANNEL DEVICES	8
	FABRICATION OF N-CHANNEL DEVICES	16
IV	INTERFACE DOPING	23
	SELECTION OF DOPANTS	23
	DOPANT CONCENTRATION	25
	DOPING CONDITIONS	25
	VACUUM DEPOSITION OF METAL DOPANTS BY EVAPORATION	26
	TUNGSTEN OXIDE EVAPORATION	30
	DOPANT DEPOSITION BY SPUTTERING	30
	DOPANT DEPOSITION BY SOLUTION DOPING	30
	ANALYTICAL PROCEDURES	31
V	WRITE CHARACTERISTICS	34
	WRITE MECHANISMS AND WRITE CURVES	34
	WRITE CHARACTERISTICS OF P-CHANNEL DEVICES	27
	Comparison with undoped devices	39
	Dependence of write speed on dopant concentration	41
	Dependence of write speed on oxide thickness	43
	Temperature dependence	43
	WRITE CHARACTERISTICS OF DEVICES DOPED BY SPUTTERING	48
	SUMMARY OF WRITE CHARACTERISTICS	48
VI	DOPANT CONCENTRATION DEPENDENCE OF MEMORY WINDOW	54

TABLE OF CONTENTS (Cont'd.)

SECTION		PAGE
VII	MEMORY RETENTION	69
	STORED CHARGE DECAY AS A FUNCTION OF TIME	69
	THE EFFECT OF OXIDE THICKNESS	72
	THE EFFECT OF DOPANT CONCENTRATION	78
	TEMPERATURE DEPENDENCE	81
	THE EFFECT OF HIGH POSITIVE APPPLIED VOLTAGES	91
	THE EFFECT OF ENDURANCE CYCLING	94
VIII	FAST SURFACE STATE GENERATION	98
	SURFACE STATE GENERATION UNDER PROLONGED BIAS	98
	SURFACE STATE GENERATION DUE TO WRITE/ERASE CYCLING	101
IX	ENDURANCE	
	DEPENDENCE OF ENDURANCE ON WINDOW BEING CYCLED	108
	DEPENDENCE OF ENDURANCE ON OXIDE THICKNESS	113
	DEPENDENCE OF ENDURANCE ON DOPANT CONCENTRATION	117
	TEMPERATURE DEPENDENCE OF ENDURANCE CYCLING	117
	ENDURANCE OF DEVICES DOPED BY SPUTTERING	111
	COMPARISON OF ENDURANCE FOR VARIOUS DOPANTS	122
X	TOTAL DOSE IONIZING RADIATION EFFECTS IN INTERFACE DOPED MNOS TRANSISTORS	127
	INTRODUCTION	127
	IRRADIATION OF STABLE GATE P-CHANNEL TRANSISTORS	129
	Comparison with undoped devices	129
	Dopant concentration dependence	129
	Dependence on gate bias	134
	Bias effects	134

TABLE OF CONTENTS (Cont'd.)

SECTION		PAGE
	IRRADIATION OF MEMORY TRANSISTORS	147
	Comparison with undoped devices	147
	Dopant concentration dependence	158
	Gate bias effects	158
	Oxide thickness effects	158
	Ability to rewrite after irradiation	169
	Memory retention after irradiation	169
	CONCLUSIONS	169
XI	PROCESS YIELD ASSESSMENT	171
	P-CHANNEL YIELD	171
	N-CHANNEL YIELD	171
	CONCLUSIONS	198
XII	CONCLUSIONS	199
	APPENDIX	205

LIST OF ILLUSTRATIONS

FIGURE		PAGE
1	Conventional vs. Interface-Doped MNOS	2
2	Stepped Oxide Varactor Wafer and Evaporated Dopant Profile	6
3	Oxide Thickness vs. Time for (100) Silicon	13
4	E-Beam Evaporation Method of Interface Doping	27
5	Top View of Wafer Holder	28
6	Auger Spectrum of Tungsten Doped Surface	32
7	Tungsten Auger Peak Amplitude vs. Quartz Crystal Coverage	33
8	Threshold Voltage Changes in Interface-Doped MNOS	35
9	Schematic of Write Characteristics	36
10	Write Characteristics of Chromium Doped P-Channel Varactors	38
11	Write Characteristic Curves of Doped and Undoped P-Channel Devices	40
12	Cr Dopant Concentration vs. Time of 25V Intersection for P-Channel Devices	42
13	Time of 25V Intersection vs. Oxide Thickness	44
14	25V Write Characteristic Curve at Elevated Temperatures	45
15	Write Characteristics of Tungsten Doped N-Channel Varactors	46
16	Write Characteristics of Platinum Doped N-Channel Varactors	47
17	Write Characteristics of Varactors Doped with Sputtered Nickel, P-Channel Varactors	51
18	Write Characteristics of P-Channel Varactors Doped with Sputtered Chromium	52
19	Platinum Saturation Memory Window vs. Dopant Concentration, P-Channel Varactors	55
20	Tungsten Saturation Memory Window vs. Dopant Concentration, P-Channel Varactors	56
21	Nickel Saturation Memory Window vs. Dopant Concentration, P-Channel Varactors	57

LIST OF ILLUSTRATIONS (Cont'd.)

FIGURE		PAGE
22	Chromium Saturation Memory Window vs. Dopant Concentration, P-Channel Varactors	58
23	Iridium Saturation Memory Window vs. Dopant Concentration, P-Channel Varactors	59
24	Palladium Saturation Memory Window vs. Dopant Concentration, P-Channel Varactors	60
25	Iridium Saturation Memory Window vs. Dopant Concentration, N-Channel Varactors	62
26	Platinum Saturation Memory Window vs. Dopant Concentration, N-Channel Varactors	63
27	Chromium Saturation Memory Window vs. Dopant Concentration, N-Channel Varactors	64
28	Niobium Memory Windows vs. Oxide Thickness, P-Channel Varactors	65
29	Memory Window vs. Tantalum Concentration, P-Channel Varactors	66
30	Molybdenum Memory Window vs. Dopant Concentration, P-Channel Varactors	67
31	Retention of Chromium Doped P-Channel Memory Device	71
32	Retention of Iridium Doped N-Channel Memory Device	73
33	Retention of Platinum Doped N-Channel Memory Device	74
34	t_R and τ_{relax} vs. Oxide Thickness, P-Channel Devices	79
35	τ_{relax} (V_{app}) vs. Dopant Concentration, P-Channel Devices	82
36	τ_{relax} (V_{app}) vs. Dopant Concentration, N-Channel Devices	83
37	Chromium Retention at Four Temperatures for P-Channel Devices	84
38	Platinum Retention at Room Temperature and 250°C for P-Channel Devices	86
39	Charge Decay at Room Temperature and 77°K for P-Channel Devices	87
40	Tungsten Retention at Three Temperatures for N-Channel Devices	88

LIST OF ILLUSTRATIONS (Cont'd.)

FIGURE		PAGE
41	Tungsten Retention at 125°C for N-Channel Devices	89
42	Tungsten Retention at 125°C for N-Channel Devices	90
43	Palladium Retention at High Positive Applied Voltages, P-Channel Devices	92
44	Platinum Retention at High Positive Applied Voltages, P-Channel Devices	93
45	Tungsten Retention at High Positive Applied Bias	95
46	Platinum Retention at High Positive Applied Bias	96
47	Platinum Retention Before and After Endurance Cycling (P-Channel)	97
48	N_{ss} Generation at High Bias for Volatges Below 20V (P-Channel)	99
49	N_{ss} Generation at High Bias for Voltages Above 20V (P-Channel)	100
50	N_{ss} Generation at High Positive Bias for Tungsten Doped P-Channel Varactors	102
51	Surface State Formation During Write Erase Cycling (P-Channel)	103
52	Memory Window Measured at Room Temperature and 77 K vs. Write/Erase Cycles (P-Channel)	104
53	Surface States vs. Write/Erase Cycling for P-Channel Devices	106
54	Memory Window Measured at Room Temperature and 77K vs. Write/Erase Cycles (N-Channel)	107
55	Endurance of Platinum Doped P-Channel Varactors	109
56	Endurance of Chromium Doped N-Channel Varactors	110
57	Endurance of Iridium Doped N-Channel Varactors	111
58	Endurance of Cr Doped P-Channel Varactors for Different Cycled Windows	112
59	Endurance of Ni Doped P-Channel Varactors for Four Cycled Windows	114
60	Endurance of Cr Doped P-Channel Varactors for Various Oxide Thicknesses	115

LIST OF ILLUSTRATIONS (Cont'd.)

FIGURE		PAGE
61	Endurance of Pt Doped N-Channel Varactors for Various Oxide Thicknesses	116
62	Endurance of Cr Doped P-Channel Varactors for Several Dopant Concentrations	118
63	Endurance Window Center Voltage vs. Dopant Concentration (P-Channel)	119
64	Endurance of Pt Doped N-Channel Varactors for Two Dopant Concentrations	120
65	Endurance of Platinum Doped P-Channel Varactors at Elevated Temperatures	121
66	Endurance of Cr Sputter-Doped P-Channel Varactors	123
67	Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Doped Devices Compared to Undoped Device	130
68	Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Comparing Effects of Different Cr Concentrations	131
69	Threshold Shift During Irradiation as a Function of Cr Concentration	132
70	Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Comparing Effects of Different Ir Concentrations	133
71	Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Effects of +10V Gate Bias on Two Cr Concentrations	135
72	Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Effects of 0V Gate Bias on Two Cr Concentrations	136
73	Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Effects of -10V Gate Bias on Two Cr Concentrations	137
74	10V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation	138
75	5V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation	139
76	-10V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation	140
77	-5V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation	141

LIST OF ILLUSTRATIONS (Cont'd.)

FIGURE		PAGE
78	Bias Effects in Cr Doped P-Channel Stable Gate Transistors During Irradiation	142
79	Gate Bias Effects in Stable Gate Ir Doped P-Channel Transistors During Irradiation	143
80	Stable Gate Threshold "Upturn" During Irradiation with Negative Gate Bias	144
81	Irradiated Stable Gate Transistor Gain, Positive Gate Bias	145
82	P-Channel Stable Gate Transistor Gain with Zero Bias During Irradiation	146
83	P-Channel Memory Window vs. Total Dose Radiation for Undoped P-Channel Transistors	148
84	Ir Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias	150
85	W Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias	151
86	Pt Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias	152
87	Pd Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias	153
88	Ni Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias	154
89	Cr Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias	155
90	Pt Doped N-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias	156
91	Comparison of Positive Threshold Decay at Zero Bias for Different Dopants During Irradiation	157
92A	Memory Window Decay During Irradiation, Low Dopant Concentration	159
92B	Memory Window Decay During Irradiation, High Dopant Concentration	159
93	Comparison of Positive Threshold Decay at 10V bias for Different Dopants During Irradiation	160

LIST OF ILLUSTRATIONS (Cont'd.)

FIGURE		PAGE
94A	Comparison of Positive Threshold Decay at 5V Bias for Different Dopants During Irradiation	161
94B	Comparison of Positive Threshold Decay at 5V bias for Different Dopants During Irradiation	161
95	Comparison of Positive Threshold Decay at -5V Bias for Different Dopants During Irradiation	162
96	Effects of Different Biases on Pd Doped, P-Channel Positive Memory Thresholds	163
97	Effects of Different Biases on Ni Doped, P-Channel Positive Memory Thresholds	164
98	Effects of Different Biases on Cr Doped, P-Channel Positive Memory Thresholds	165
99	Effects of Different Biases on Pt Doped, P-Channel Positive Memory Thresholds	166
100	Effects of Different Biases on Pt Doped, N-Channel Positive Memory Thresholds	167
101	Memory Window Decay During Irradiation for Devices with Different Oxide Thicknesses	168
102	Accelerated Retention Tests Performed on Pt Doped, P-Channel Transistors After a Total Dose of 3×10^6 Rads (Si)	170
103	Chromium Doped N-Channel Varactor Yield	173
104	Platinum Doped N-Channel Varactor Yield	174
105	Iridium Doped N-Channel Varactor Yield	175
106	Yield Survey Map of Chromium Doped N-Channel Memory Transistors	176
107	Yield Survey Map of Platinum Doped N-Channel Memory Transistors	177
108	Yield Survey of Device Characteristics on Wafer AE28-9A, Stable Gate and Memory Devices	182-5
109	Yield Survey of Device Characteristics on Wafer A28-9B, Stable Gate and Memory Devices	186-9
110	Yield Survey of Device Characteristics on Wafer A28-9C, Stable Gate and Memory Devices	190-3

LIST OF ILLUSTRATIONS (Cont'd.)

FIGURE		PAGE
111	Yield Survey of Device Characteristics on Wafer A28-9D, Stable Gate and Memory Devices	194-7
112	Charge Accumulation in CaF_2:MnO Thermoluminescent Dosimeters During Co^{60} and Electron Beam Irradiation as a Function of Total Dose Radiation	207

LIST OF TABLES

TABLE		PAGE
1	MNOS Memory Transistor Fabrication Sequence - Phase I	8
2	Oxide Growth vs. Time for T = 1050°C	14
3	n-MNOS Stable Gate and Memory Transistor Fabrication Sequence	16
4	Reactivities of Potential Dopants	24
5	Multipliers to Calculate Dopant Concentration	29
6	Write Parameters for P-Channel Memory Devices	49
7	Write Parameters for N-Channel Memory Devices	50
8	Retention Parameters for the Six Dopants, P-Channel Devices	75
9	Retention Parameters for the Three Dopants, N-Channel Devices	77
10	Variation of Decay Slope with Concentration	80
11	Variation of "b_R" with Dopant Concentration	80
12	Endurance Parameters for P-Channel Devices	124
13	Endurance Parameters for N-Channel Devices	126
14	Results of Yield Survey of Polysilicon Stable Gate N-Channel Transistor	179
15	Important Process Parameters for Wafer Run #9	180
16	Device Yields for Wafer Run #9	180
17	Endurance x Retention Product	200
18	Optimum Devices	202

SECTION I

INTRODUCTION

Interface doping of dual dielectric charge storage cells of the IGFET types was introduced by Kahng et al[1] and Thornber et al[2] in 1974. In this method, a layer of metal, such as tungsten, usually less than a monolayer thick, is placed between a thin silicon dioxide film (first dielectric), which is grown to a thickness of the order of 100A thick on silicon, and an alumina or silicon nitride film (second dielectric), which is of the order of 400A thick. This was followed by an aluminum film, to make up the MAOS or MNOS structure. It was established by Kahng et al that the dopants act as trapping sites for charge injected from the silicon. Charge is injected into these sites from the silicon under the influence of a high applied field. Here the charge motion mechanism is by Fowler-Nordheim tunneling, rather than by direct tunneling, which is the mechanism which operates for the conventional, thin oxide dual dielectric storage cells (Fig. 1). The principal differences between the conventional MNOS and the interface doped MNOS device are:

1) The stored charge is separated from the silicon by a much thicker oxide film,
2) The stored charge resides principally at the dopant sites, and not 100-200A inside the nitride film, as it does in the conventional MNOS.
3) The stored charged consists principally of "excess" electrons.

---

[1] D. Kahng, W. J. Sundburg, D. M. Boulin, and J. R. Ligenza, Bell System Technical Journal, Vol. 53, 1974, p. 1723.

[2] K. K. Thornber, D. Kahng, and C. T. Neppell, Bell System Technical Journal Vol. 53, 1974, p. 1741.

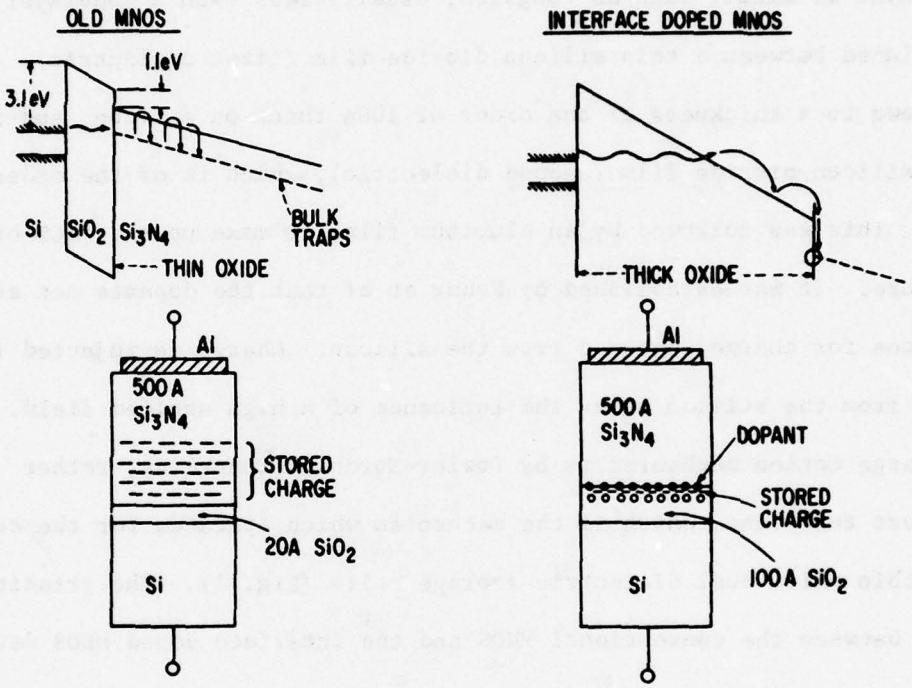


Figure 1. Conventional vs. Interface-Doped MNOS

This has the following important consequences:

1) The stored charge is retained for very long times.
2) The cell is very insensitive to read-disturb.
3) Device degradation mechanisms associated with charge motion in the nitride are less important.
4) The memory window, i.e., the separation between the two threshold voltages corresponding to the two memory states, is predominantly positive.

The charge retention in interface-doped MAOS devices has been studied extensively by Thornber et al[2]. It was found by them that charge loss could be accelerated at elevated temperatures and applied bias voltages; the extrapolated charge retention was 500 years at 80°C. The charge decay mechanism at temperatures between 150 to 300°C was found to be by activated conduction through the alumina to the gate electrode.

In this previous work, emphasis was placed on tungsten as the interface dopant and alumina as the second dielectric, although other dopants such as Pt, Ta, Ir, and silicon nitride as the second dielectric were also explored. A lower limit of the doping concentration of 10^{14} cm^{-2} and an upper limit of $5 \cdot 10^{15}$ cm^{-2} was identified. Device endurance toward write/erase cycling was not reported.

The work reported here is an investigation of interface doping in both n- and p-channel MOS devices. Specifically, we describe the use of ten different interface dopant metals in MNOS memory varactors and transistors.

Included are the write/erase characteristics as a function of the dopant concentration and oxide thickness, memory window as a function of dopant concentration and oxide thickness, write speeds as a function of write pulse width and amplitude, the charge retention as a function of doping

concentration and oxide thickness, the endurance toward write/erase cycling. radiation hardness toward total dose ionizing radiation, and yield assessment.

In the first phase of this investigation, only p-channel devices were fabricated and tested. In the second phase, the work was extended to n-channel devices. However, the number of dopants in the second phase was limited to Pt, Cr, Ir and W. In addition, the total dose radiation hardness of interface doped devices was investigated during the second phase. This work involved the exposure of interface doped transistors, both memory and stable gate, to increasing Co^{60} radiation levels at various bias voltages on the gate. This work concentrated on p-channel transistors, although some data on n-channel memory transistors were also obtained. Finally, a yield assessment was made using simulated array processing to ascertain the effect on yield due to interface doping.

Interface doped MNOS memory devices offer the potential for short write and erase times, as well as very long retention. From circuit considerations, it is desirable that the memory transistor always be in the "off" or non-conducting state, to avoid the necessity of an additional transistor for each memory cell. Since the interface doped memory device tends to store "excess" electrons rather than holes, it follows that the memory window, which is the separation between the threshold voltages corresponding to the two binary memory states, is predominantly positive , the center voltage being typically +5V. It is consequently the n-channel device which has the memory window predominantly in the non-conducting (positive) gate potential region, thus giving larger memory windows. In the second phase of this work, all fabrication and testing was shifted to n-channel devices.

The endurance of all devices fabricated in this program, p- or n-channel, did not exceed 10^7 write/erase cycles. Therefore, attempts to fabricate RAM devices were dropped.

SECTION II

APPROACH

A survey of the various dopants and oxide thicknesses was made during the first phase of this work using p-channel varactors. In order to survey as many dopant concentrations and oxide thicknesses as quickly as possible and without interference from processing artifacts, a large number of varactor cells of varying concentrations and oxide thicknesses were prepared on a single silicon wafer. This was accomplished by preparing 5 to 6 oxide stripes across the wafer of increasing thickness (usually from 50 to 140A) by alternate thermal growth and subsequent partial removal of the oxide film by etching. This gives rise to a step pattern in the oxide thickness. The interface dopant is now deposited in such a way that its concentration varies from zero on one end of the wafer to a pre-determined level such as 10^{15} or 10^{16} cm^{-2} on the other, giving a wedge-like thickness distribution in between. The dopant concentration gradient is perpendicular to the oxide thickness gradient, thus giving a full range of dopant concentrations with each oxide thickness. In practice, this method is applicable if the variation in the doping concentration does not greatly exceed one order of magnitude. As a result, a concentration range of about one order of magnitude and six oxide thicknesses can be evaluated on one wafer. This is illustrated in Fig. 2.

From this survey on p-channel varactors, a selection of the six most promising dopants was made, as well as the most suitable oxide thickness for EAROM devices. Processing of both p-channel and n-channel transistors was then limited to these dopants and thickness. The number of promising dopants was still further limited for the fabrication of n-channel varactors and transistors.

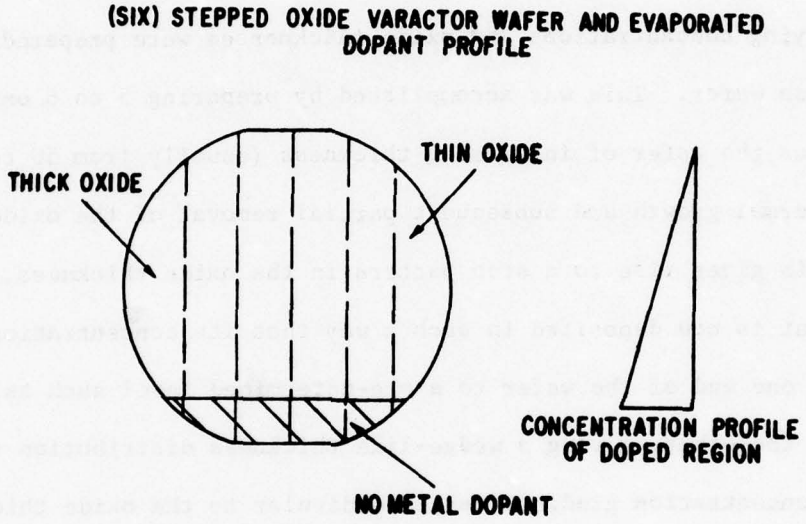


Figure 2. Stepped Oxide Varactor Wafer and Evaporated Dopant Profile

Accelerated test methods were used wherever possible. Thus, to measure charge retention after writing, high gate bias voltages were applied to force an observable charge decay within several minutes. Extrapolation to zero bias voltage gives the expected retention under real use conditions. Since the endurances measured in this program have not exceeded 10^7 cycles, accelerated measurements have not been necessary.

In order to properly assess the effect of interface doping, each processed wafer had a control region which was identical in all respects to the rest of the wafer except that it was not interface doped. In addition, process control wafers were added at various stages to measure oxide and nitride thickness and the nitride refractive index.

SECTION III

INTERFACE-DOPED MNOS DEVICE FABRICATION

In this section, the MNOS processes used to fabricate both p- and n-channel interface doped varactors and transistors are described.

FABRICATION OF P-CHANNEL DEVICES

P-channel devices were processed on 2 inch silicon wafers of (100) orientation, having 3 to 8 Ω-cm n-type resistivity (phosphorus). Aluminum gates are used.

The general MNOS fabrication sequence used for p-channel memory transistors, including stable gate transistors, is shown in Table 1. For varactors, steps 2 through 8, 12 through 14, and 17 are omitted. All these steps are described below.

TABLE 1

MNOS MEMORY TRANSISTOR FABRICATION SEQUENCE -- PHASE I

Step No.	Description
1	Initial cleaning
2	Wafer oxidation
3	Source drain mask
4	Source drain predeposition
5	Source drain drive-in
6	Stable gate mask
7	Stable gate oxide
8	Memory gate mask
9	Memory gate oxidation
10	Interface doping
11	Nitride deposition

Step No.	Description (contd.)
12	Oxide deposition (SiO_2)
13	Contact mask (SiO_2)
14	Nitride oxide etch
15	Metal deposition
16	Interconnection mask
17	Interconnection sinter

(1) Initial cleaning

The initial cleaning process removes any surface contaminants that may remain on the wafers in the as-received condition.

The silicon wafers are first immersed in a 50/50 mixture of hydrofluoric acid (HF) and deionized water. They are next rinsed with deionized water and blown dry with nitrogen. In a quartz tube furnace at 1050°C, a thermal oxide is grown on the wafers. With pure oxygen flowing at 1 cubic ft./hr., 30 minutes is sufficient to grow a layer 180Å thick. At this point, the dilute hydrofluoric acid bath is repeated. The oxide layer and any trapped impurities are stripped away. The cleaning step ends with a final rinse in deionized water and drying with nitrogen.

(2) Wafer oxidation

Wafer oxidation occurs in two parts. First a layer of thermal oxide 1100Å thick is grown on the wafers in the manner described in step 1. At 1050°C and an oxygen flow rate of 1 cubic ft/hr, three hours are needed.

Second, 5200Å of SiO_2 are deposited on the wafers by chemical vapor deposition in a silox reactor. The silox reactor is purged for 15 minutes with line nitrogen. During this time, the heater block in the furnace is heated to 450°C. After the purge, the line nitrogen is turned off. Bottled nitrogen, oxygen and silane (SiH_4) diluated in argon flow through the reactor tube at

the rates listed below:

Oxygen	0.211 liters/min.
Nitrogen	0.066 "
5.4% SiH_4 in Argon	0.45 "

After thus clearing the gas feed lines, the silane-in-argon is vented directly to the exhaust, and the oxygen is turned off. At this time,the wafers are inserted into the reactor. During a two-minute nitrogen purge, the wafers heat to the reaction temperature. The furnace now automatically begins a deposition run. Twelve minutes at the specified flow rates is sufficient to deposit 5200 Å of SiO_2. Thickness is determined by referring to a color/thickness table.

The 6300 Å (total thickness) of SiO_2 will act as a diffusion stop during the source/drain diffusion.

One of the by-products of the silox reaction is water vapor. Because of the harmful effect of water on photoresist, the wafers are baked for 30 minutes at 175°C in a nitrogen atmosphere prior to the next step.

(3) Source drain mask

The diffusion stop SiO_2 layer must be etched in this step to expose the source drain regions of the wafers. Photoresist is spun on to the wafers at 5000 rpm with a photoresist spinner. The resist is dried for 30 minutes in a nitrogen atmosphere at 80°C. The source-drain mask is then aligned on the wafers and the wafers are exposed to ultraviolet light. Resist developer is now used to wash away the photoresist that was not exposed to the UV light at the source and drain regions. The wafers are now baked for 30 minutes in a nitrogen atmosphere at 175°C in preparation for the oxide etching step. The etchant is composed of 1 part hydrofluoric acid and 9 parts NH_4F. Three minutes are sufficient to remove the oxide above the source and drain without appreciable undercutting of the photoresist. After rinsing in deionized water,

the remaining photoresist is removed in microstrip heated to 95°C (5 minutes) and boiling deionized water (3 minutes). Finally, the wafers are cleaned in a vapor degreaser with a solvent mixture of equal parts of isopropyl alcohol, acetone and trichlorethylene and blown dry with nitrogen.

Periodic microscope checks are made during this step to insure correct alignment and proper etching.

(4) Source drain predeposition

The p-dopant which we use is boron. The wafers to be doped are arranged vertically in a quartz rack, interspersed with wafers of boron nitride. The rack is then inserted into a tube furnace (1000°C) with a nitrogen atmosphere for 15 minutes. Boron is transferred to the silicon wafers, where a thin layer of silicon at the source and drain regions becomes very highly doped.

(5) Source drain drive-in

Before the boron dopant is driven into the silicon surface, the silicon dioxide and boron residing on wafer surfaces are stripped away in 50/50 HF. The wafers are then inserted into the 1000°C tube furnace for 3 hours in oxygen. The junction depth is about 1.5 microns. Simultaneously, 1100 Å of thermal oxide are grown on the wafers.

(6) Stable gate mask

Fifty-two hundred Å of SiO_2 are again depcsited on top of the thermal oxide layer. This oxide layer, which totals 6300 Å, is masked and etched to give the stable gate mask pattern.

(7) Stable gate oxidation

The stable gate oxide, which is 500Å thick, is a thermal oxide grown at 1000°C for 1½ hrs with an oxygen flow of 1 cu. ft/hr.

(8) Memory gate mask

In the great majority of our devices, the stable gate oxide was not used.

In these cases, the stable gate mask served to expose the memory region. Those wafers which had stable gates, however, employed a memory gate mask for the thinner memory oxide.

(9) Memory gate oxide

The memory gate oxides ranged in thickness from 30Å to 134Å. They were grown in a tube furnace at 1050°C. To more closely control the growth process, the flow gas is 1% oxygen in argon. Figure 3 shows the relationship between oxide thickness and time.

(9a) Memory gate oxide varactors used in survey phase

For much of the initial survey of interfacial dopants, varactors were used instead of transistors because of their much more rapid producibility. The use of varactors enables us to vary the gate oxide thickness within a single wafer, further minimizing the effect of wafer-to-wafer differences, as illustrated in Fig. 2. It required oxidizing the wafers 6 separate times. After each oxidation, the wafers were partly immersed in 50/50 HF and water to remove a portion of the oxide layer. For instance, after the first gate oxidation, all but the leftmost strip of the wafer would remain. Table 2 contains the thickness vs. total oxidation time data for one particular six step oxide run.

(10) Interface doping

This important process step is covered in section IV.

(11) Nitride deposition

Silicon nitride is deposited in an epitaxial reactor by the SiH_4/NH_3 reaction at a wafer temperature of 850°C. The reactor is first given a 10 minute nitrogen purge. During this time, the silane, ammonia and hydrogen flow rates are set. The ratio of silane to ammonia is 1/1000. After the purge, the wafers are inserted into the reactor and brought to temperature in

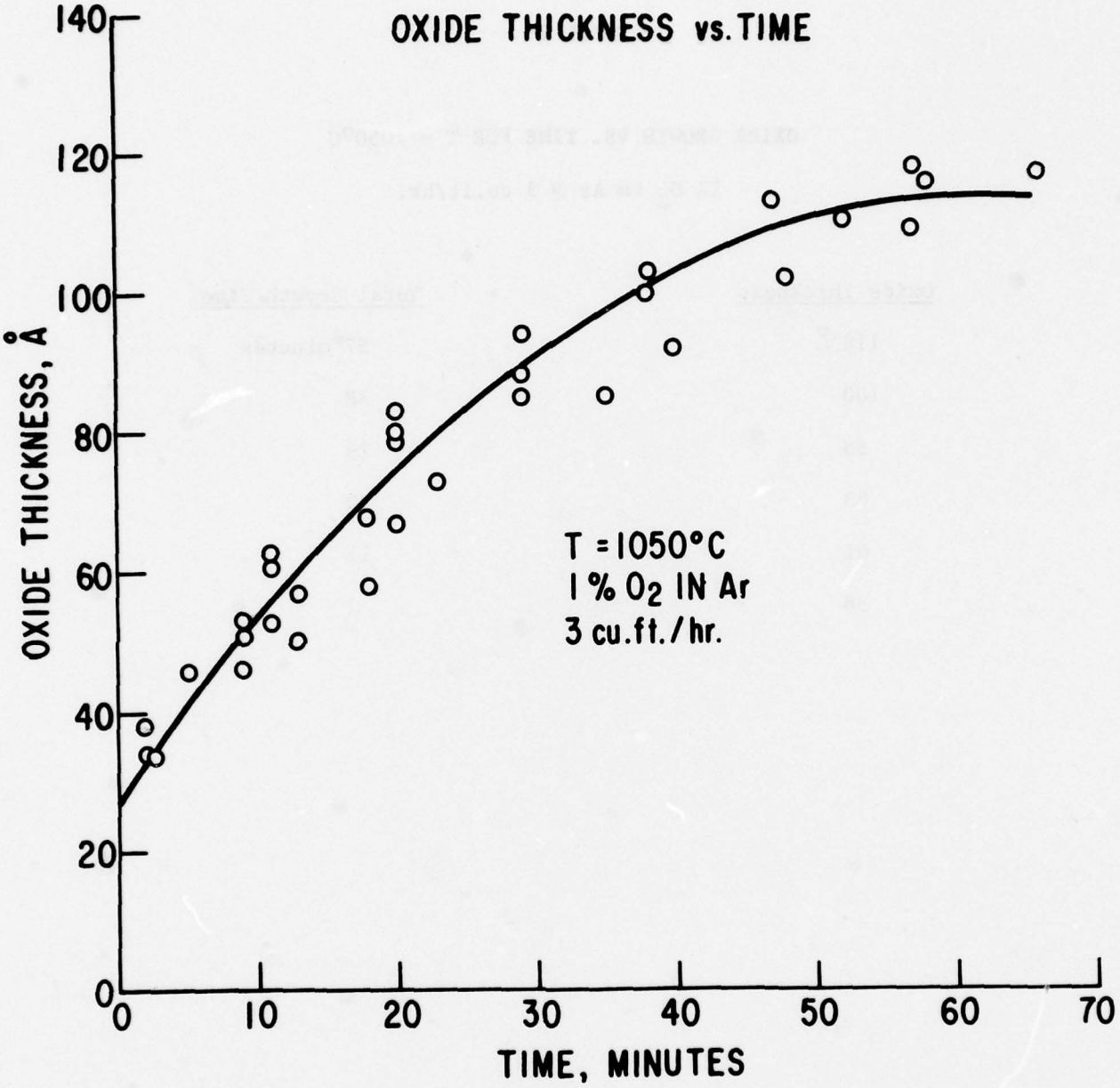


Figure 3. Oxide Thickness vs. Time for (100) Silicon

TABLE 2

OXIDE GROWTH VS. TIME FOR T = 1050°C

1% O_2 in Ar @ 3 cu.ft/hr.

Oxide Thickness	Total Growth Time
118 Å	57 minutes
100	38
88	29
83	20
61	11
38	2

the presence of the hydrogen flow gas. Fast write devices have a nitride thickness in the neighborhood of 300Å, and most slow write devices have 450 - 600 Å nitride layers. Deposition times are from 1/2 min. to 1 min. long.

(12) Oxide deposition (SiO_2)

For a third time, 5200Å of SiO_2 are deposited by the chemical vapor method. This oxide will remain on the wafers as a field oxide.

(13) Contact mask

This mask allows windows to be etched down to sources and drains, so that they can be contacted with aluminum, which will be deposited in a later step.

(14) Nitride oxide etch

The 5200Å of oxide are first etched by immersing the wafers for three minutes in buffered HF (NH_4F/HF:9/1) as described earlier. The photoresist is removed and wafers cleaned, degreased and dried. The wafers are then boiled for 45 minutes in phosphoric acid to etch the nitride layer.

(15) Metal deposition

An aluminum layer is deposited by electron beam evaporation. The wafers are placed in a bell jar which is evacuated to 10^{-6} torr. An aluminum slug is melted with an electron beam and the wafers are coated to a thickness of 1 to 1.5 μm. The thickness is monitored by quartz crystals.

(16) Interconnection mask

Photoresist is patterned on the wafers as before, using the interconnection mask. The aluminum is etched in a solution of 76% phosphoric acid, 15% acetic acid, 5% water, and 4% nitric acid heated to 45°C. Etching time is 1 to 2 minutes. The photoresist is stripped and the wafers are again boiled in deionized water and vapor degreased.

(17) Interconnection sinter

Processed wafers are annealed at 500°C for 25 minutes in an annealing

oven. Nitrogen and hydrogen are used at the following flow rates:

Nitrogen - 2 cubic ft/hr.

Hydrogen - 0.1 cubic ft/hr.

FABRICATION OF N-CHANNEL DEVICES

N-channel devices were processed on 2 inch silicon wafers of (100) orientation, having 2 Ω-cm p-type resistivity (boron). Stable gate devices possess polysilicon gates. All memory devices are aluminum gate.

The general MNOS fabrication sequence used for n-channel stable gate and memory transistors is shown in Table 3. All steps are described below.

TABLE 3

n-MNOS STABLE GATE AND MEMORY TRANSISTOR FABRICATION SEQUENCE

Step No.	Description
1	Initial cleaning
2	Surface doping
3	Wafer oxidation
4	Source drain mask
5	Stable gate oxidation
6	Polysilicon deposition
7	Polysilicon stable gate mask
8	Polysilicon doping
9	Preferential etch
10	Source drain predeposition
11	Source drain drive-in
12	Memory gate mask
13	Memory gate oxidation
14	Interface doping
15	Nitride deposition

Step No.	Description (contd)
16	Oxide deposition (SiO_2)
17	Contact mask (SiO_2)
18	Nitride oxide etch
19	Metal deposition
20	Interconnection mask
21	Interconnection sinter

(1) Initial cleaning

The initial cleaning process is the same as that described on page 9 for p-MNOS device fabrication.

(2) Surface doping

The tendency of the surface of a lightly doped n-type wafer to invert makes n-channel MOS transistors prone to become depletion devices. This can be avoided by doping the surface of the wafer somewhat heavier with boron than the interior of the wafer. In this way, enhancement devices are obtained without adding greatly to the junction sidewall capacitance.

The p-type wafers used in the fabrication of n-channel MNOS devices in this program have an initial sheet resistivity of about 80 $\Omega/\square$. Surface doping by boron decreased this value to about 75 $\Omega/\square$. This results in enhancement devices with a threshold voltage of around 1.5 V.

Because of the heavier surface doping, and the associated higher defect density compared to the undoped case, there was a reduction of the mobility. The mobility with surface doping is approximately 200 $cm^2/V\text{-sec}$. Although this is less than one-half that obtained without doping, it is a necessary trade-off to obtain higher threshold voltages.

The 5 $\Omega/\square$ decrease in sheet resistivity is achieved by arranging the wafers vertically in a quartz rack, interspersed with wafers of boron nitride.

The rack is then inserted into a tube furnace (1000°C) with a nitrogen atmosphere (0.5 cubic ft/hr) for 90 seconds.

(3) Wafer oxidation

Wafer oxidation occurs in two parts. Approximately 1000Å of thermal oxide (SiO_2) are grown in a quartz tube furnace at 1050°C. Pure oxygen flows through the furnace at 0.5 cubic ft/hr. Time required is 1.5 hrs.

Second, 5200Å of SiO_2 are deposited on the wafers by chemical vapor deposition in a silox reactor. This procedure is described on page 9, step 2.

(4) Source-drain mask

The source-drain regions for stable and memory devices are opened in the 1000Å oxide layer deposited in the previous step. After baking the wafers at ~ 180°C, a negative photoresist is spun on to the wafers at 6000 rpm for 10 seconds with a phororesist spinner. The resist is dried for 20 minutes in a nitrogen atmosphere at 65°C. The source-drain mask is then aligned on the wafers and the wafers are exposed to ultraviolet light (4 seconds). Resist developer is now used to wash away the photoresist that was not exposed to the UV light at the source and drain regions. The wafers are now baked for 20 minutes in a nitrogen atmosphere at 135°C in preparation for the oxide etching step. The etchant is composed of 1 part hydrofluoric acid and 9 parts NH_4F. Three minutes are sufficient to remove the oxide above the source and drain without appreciable undercutting of the photoresist. After rinsing in deionized ater, the remaining photoresist is removed in microstrip heated to 95°C (5 minutes) and warm acetone (5 minutes). Finally, the wafers are boiled in an isopropyl alcohol bath (10 minutes), rinsed in deionized water, and blown dry with nitrogen.

Periodic microscope checks are made during this step to insure correct

alignment and proper etching. The source and drain contacts for the stable gate devices are self-aligning, that is, the source and drain regions and the gate region between them are etched simultaneously and, in later steps, the polysilicon gates will act as masks during the doping step.

(5) Stable gate oxidation

Another 1000Å thick layer of thermal oxide is grown on the wafers in the manner described in step (3). This layer will act as the stable gate oxide.

(6) Polysilicon deposition

The polysilicon gate material is obtained through pyrolysis of dichlorosilane. This takes place in a hot wall furnace. The wafers are set on a quartz rack, inserted into the reaction region and heated to 853°C. After a 5 minute nitrogen purge, 0.32 ℓ/min. of dichlorosilane ($SiCl_2H$) diluted in 40ℓ/min. of nitrogen is admitted. In 10 minutes, approximately 8000Å of polysilicon are deposited. Another short purge follows and wafers are withdrawn.

(7) Polysilicon stable gate mask

The polysilicon gate regions are defined by depositing ~5000Å of silox on top of the polysilicon, patterning the oxide with a mask of the gate regions and doping the surface of the exposed gates with boron. This selective doping will permit a preferential etchant to remove the undoped polysilicon in later steps. Silox is deposited as in step (3) and is patterned as in step (4).

(8) Polysilicon doping

The surface doping of the polysilicon with boron takes place as in step (2), but the predeposition time is increased to 7 minutes. After predeposition, the silox is stripped in buffered hydrofluoric acid.

(9) Preferential etch

The undoped polysilicon is preferentially etched in 4N potassium hydroxide, heated to $\sim 65^{\circ}C$. Etch time is typically 2 to 3 minutes. Wafers are then rinsed in deionized water and then subjected to a buffered HF etch during which the source-drain contacts are cleaned. A rinse in deionized water is followed by a nitrogen blow dry.

(10) Source-drain predeposition

The n-dopant used is phosphorus. The wafers to be doped are arranged vertically in a quartz rack, interspersed with PH_3 wafers. The rack is then inserted into a tube furnace ($1000^{\circ}C$) with a nitrogen atmosphere (0.5 cubic ft/hr) for 15 minutes. Phosphorus is transferred to the silicon wafers, where a thin layer of silicon at the source and drain regions becomes very highly doped.

(11) Source drain drive in

The wafers are inserted into the $1000^{\circ}C$ tube furnace for 1.5 hours. Pure oxygen is admitted at 0.5 cubic ft/hr. As the phosphorus is driven into the source and drain, $\sim$ 1000Å of the thermal oxide are simultaneously grown.

When the diffusion is complete, all the oxide is removed from the wafers in buffered HF acid. All that remains on the wafer surfaces are the polysilicon gates and the gate oxide directly beneath them.

(12) Memory gate mask

As in step (3), 1000Å of thermal oxide and $\sim$ 5000Å of silox are deposited on the wafers. This oxide layer is then masked so as to reveal the gate regions of the (aluminum gate) memory devices.

(13) Memory gate oxidation

The memory gate oxides ranged in thickness from 50Å to 90Å. They are

grown in a tube furnace at 1050°C. To more closely control the growth process, the flow gas is 1% oxygen in argon. Figure 3 shows the relationship between oxide thickness and time.

(14) Interface doping

This important process step is covered in section IV.

(15) Nitride deposition

Silicon nitride (Si_3N_4) is deposited via the pyrolysis of ammonia and dichlorosilane at 800°C in a hot wall reactor. The wafers are placed on a quartz rack and inserted into the reaction region. After a 10 minute nitrogen purge, 200 sccm of ammonia are admitted. The nitrogen carrier gas flow rate is 50 ℓ/m. After one minute, 20 sccm of $SiCl_2H$ are added to the flow and nitride deposition takes place. Approximately 350A are deposited in 2.5 minutes. Ammonia flow is maintained for one minute after the $SiCl_2H$ flow ceases. A 5 minute nitrogen purge follows and the wafers can then be removed.

(16) Oxide deposition (SiO_2)

For a fourth time, 5200Å of SiO_2 are deposited by the chemical vapor method. This oxide will remain on the wafers as a field oxide.

(17) Contact mask

This mask allows windows to be etched down to sources and drains, so that they can be contacted with aluminum, which will be deposited in a later step.

(18) Nitride oxide etch

The 5200Å of oxide are first etched by immersing the wafers for three minutes in buffered HF (NH_4F/HF:9/1) as described earlier. The photoresist is removed and wafers cleaned, degreased and dried. The wafers are then boiled for 30 minutes in phosphoric acid to etch the nitride layer. A

deionized water rinse follows as does a nitrogen dry.

(19) Metal deposition

An aluminum layer is deposited by electron beam evaporation. The wafers are placed in a bell jar which is evacuated to 10^{-6} torr. An aluminum slug is melted with an electron beam and the wafers are coated to a thickness of 1 to 1.5 μm. The thickness is monitored by quartz crystals.

(20) Interconnection mask

Photoresist is patterned on the wafers as before, using the interconnection mask. The aluminum is etched in a solution of 76% phosphoric acid, 15% acetic acid, 5% water, and 4% nitric acid heated to 45°C. Etching time is 1 to 2 minutes. The photoresist is stripped and the wafers are again boiled in deionized water and varpor degreased.

(21) Interconnection sinter

Lastly, the wafers are annealed in nitrogen for 20 minutes at 450°C.

SECTION IV

INTERFACE DOPING

The interfacial doping step is carried out after the memory gate oxidation. In this section the selection of dopants, dopant concentration, and doping conditions are given.

SELECTION OF DOPANTS

In the selection of dopants, the following criteria were applied:

- The vapor pressure of the element or its oxide must be negligible at 850°C.
- The diffusion coefficient of the dopant at 850°C in SiO_2 or Si_3N_4 must be low.
- The dopant must not be subject to ionic motion in SiO_2 or Si_3N_4 under bias temperature stress.
- The melting point of the deposited species must be above 900°C.
- Depositing reproducibly must not be too difficult.

These criteria eliminate the alkali and alkaline earth metals because of their high ionic mobility, Au, Ag, and Cu, which have high diffusivities in SiO_2, Zn, Cd, Hg, Ga, and In, because of high vapor pressures or low melting points. Primarily the elements in group VII, I-VIIB, the rare earth elements and perhaps Al remain. The reactivities of some of those elements are given in Table 3. They fall into four classes, according to their oxide-free energy of formation:

- Elements that will not oxidize on exposure to air (Ru, Rh, Pd, Os, Ir and Pt).
- Elements that oxidize in air but can be readily reduced by hydrogen at 850°C (V, Cr, Mo, W, Fe, Co, and Ni).

- Elements that oxidize in air and are not reducible by hydrogen at 850°C (Nb and Ta).
- Elements that react with SiO_2 to form the oxide, reduce the SiO_2 to form Si (Y, Ti, Zr, and La), and are not reducible by hydrogen at 850°C.

TABLE 4

REACTIVITIES OF POTENTIAL DOPANTS

Element	Group	Oxidizes in Air	Oxide Reducible in H_2	Reduces SiO_2
La	III B	Yes	No	Yes
Ti	IV B	Yes	No	Yes
Zr		Yes	No	Yes
V	V B	Yes	Yes	No
Nb		Yes	No	No
Ta		Yes	No	No
Cr	VI B	Yes	Yes	No
Mo		Yes	Yes	No
W		Yes	Yes	No
Fe	VII	Yes	Yes	No
Co		Yes	Yes	No
Ni		Yes	Yes	No
Ru		No	--	--
Rh		No	--	--
Pd		No	--	--
Os		No	--	--
Ir		No	--	--
Pt		No	--	--

At least one metal was included from each of these classes for the initial survey phase. The metals in the fourth class will react to give a layer of metal oxide. For the initial survey, the following elements were selected: Ir, Pd, Pt, Nb, Ta, W, Mo, Cr, Ni, and Ti.

DOPANT CONCENTRATION

It is of interest to calculate the charge stored in a MNOS device to give a threshold shift of ΔV_T, if the charge is located near the silicon/insulator interface. This situation is given by:

$$Q_{stored} \cong C_o \Delta V_T$$

where C_o is the gate insulator capacitance. For ΔV_T = 10 volts, $Q_{stored} \cong$ $1.6 \times 10^{-10} C/cm^2$, or about 10^9 electronic charges/cm^2.

Kahng et al[1] have indicated that the effective doping range for tungsten in thick oxide MNOS devices was between 10^{14} to $5 \cdot 10^{15}/cm^2$. There are then 10^5 to 10^6 available dopant sites for each stored charge.

In the survey phase of this work, dopant concentrations ranged between 0 and 5×10^{16} cm^{-2}. For the fabrication of transistors in the subsequent phases of this work, dopant concentrations were kept in the 10^{14} to 5×10^{15} cm^{-2} region.

DOPING CONDITIONS

Methods that have the potential of introducing precise amounts of dopant are:

a. Vacuum deposition by evaporation or sputtering.

b. Adsorption of metal ions from solution.

c. Electroplating by current flow through the thin oxide.

d. Exposure to a gas bearing the dopant at high temperature or in electrical discharge.

e. Growing the last portion of the oxide film in the presence of small additions of dopants to the flow gas.

f. Ion implantation.

Doping by vacuum deposition, sputtering, and adsorption from solution were employed in this investigation.

VACUUM DEPOSITION OF METAL DOPANTS BY EVAPORATION

Vacuum deposition of the metal dopants is the most generally applicable technique available. Evaporation by electron gun is readily controlled and the use of quartz crystal monitors provides a reliable relative thickness standard.

Figures 4 and 5 are schematics of the deposition equipment. Figure 4 indicates the relationship between the wafer holder, the Sloan 180^{o} electron gun, the flying shutter, and the two quartz crystal monitors. Figure 5 is a top view of the wafer holder. The open and closed shutter positions are shown by the dotted lines.

The wafer holder has a capacity of four-two inch wafers. However, only during the deposition of aluminum does it hold more than 2 wafers. During a dopant evaporation only two wafers are placed at the points marked A and B in Figure 5. The darkened areas indicate the position of shields used to prevent deposition on those portions of the wafers. A small slug of the dopant metal is placed in the electron gun and the system evacuated to below 10^{-5} torr. The shutter covers the wafers and the inner oscillator.

The dopant metal is slowly heated to its melting point by the magnetically focused electron beam. The water cooled outer oscillator monitors the gradually increasing rate of evaporation.

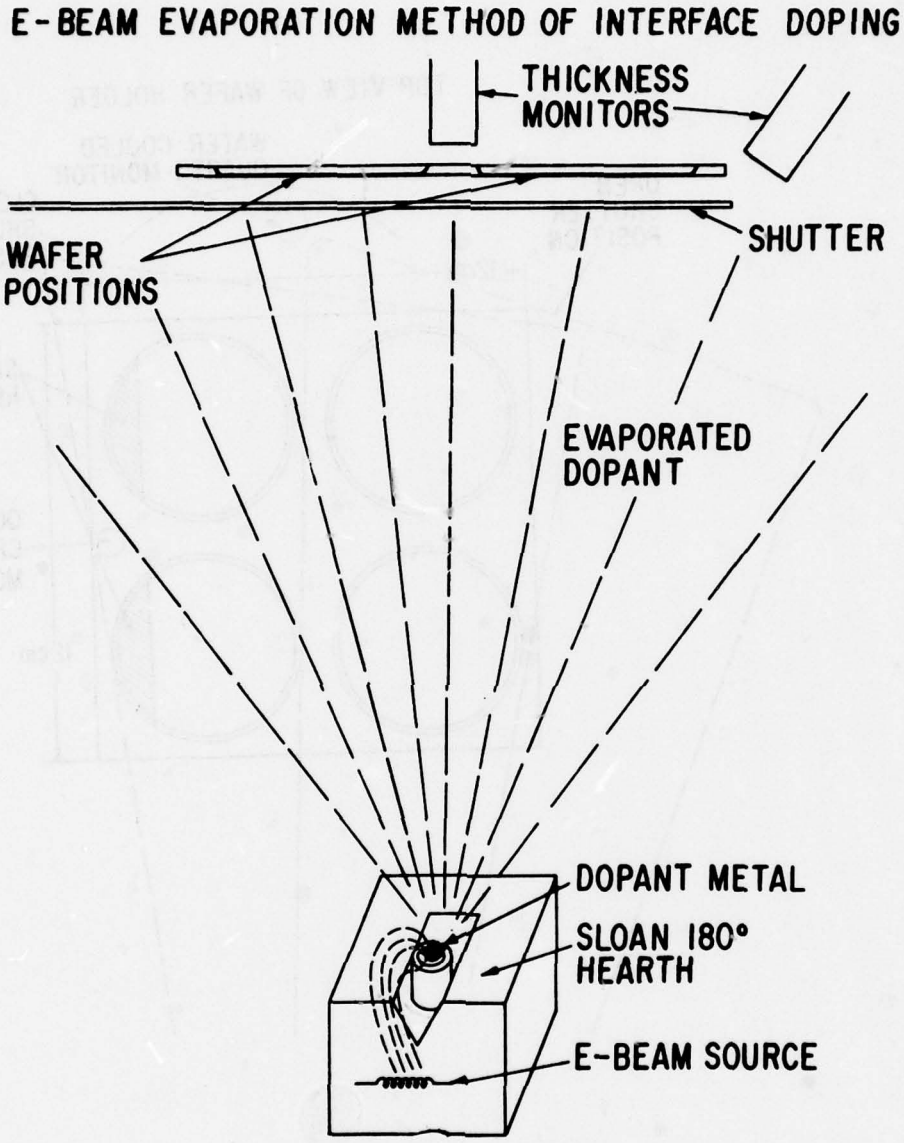


Figure 4. E-Beam Evaporation Method of Interface Doping

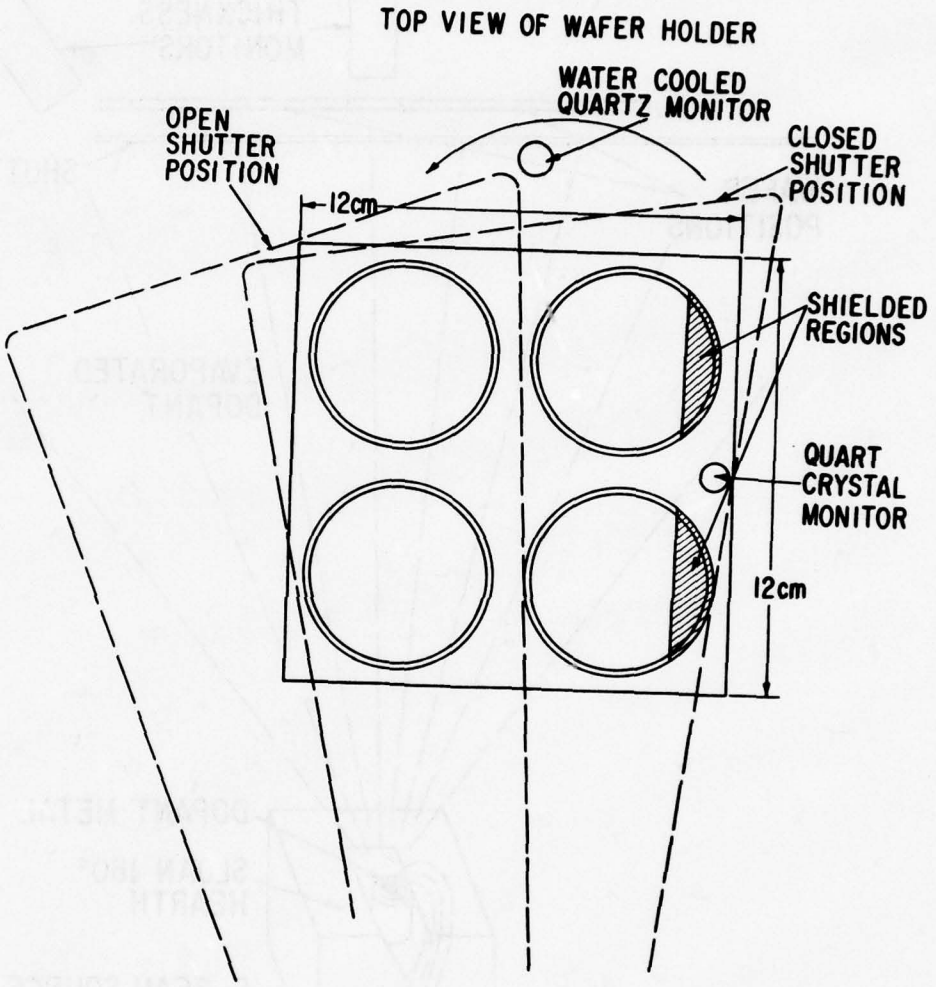


Figure 5. Top View of Wafer Holder

Once this rate has stabilized at a predetermined level, the shutter begins to open. If the rate of evaporation of a metal is high or a low dopant concentration is desired, the shutter is set to turn through the 27 degrees necessary to expose the wafers completely in 1 second. For lower evaporation rates, the shutter is allowed 5 seconds to rotate through this angle. As the shutter opens, the inner oscillator measures the evaporated metal thickness. By noting the oscillator frequency before the shutter opens and after it closes again, we can calculate the amount of dopant on those parts of the wafers exposed for the longest time.

When the wafers have been fully exposed (save for the shielded regions), the shutter is released from motor control and swings shut instantly.

Table 4 shows the multipliers necessary to calculate dopant concentration from the frequency change of the oscillator recorded during the evaporation.

TABLE 5

MULTIPLIERS TO CALCULATE DOPANT CONCENTRATION

Dopant	Maximum Dopant Concentration, x 10^{15} cm^{-2}
Tungsten	0.0717 x Δf
Iridium	0.0686 x Δf
Palladium	0.1236 x Δf
Platinum	0.0674 x Δf
Niobium	0.1416 x Δf
Tantalum	0.0724 x Δf
Molybdenum	0.1369 x Δf
Chromium	0.2536 x Δf
Nickel	0.2252 x Δf
Titanium	0.2740 x Δf

TUNGSTEN OXIDE EVAPORATION

Of the six most promising dopants, tungsten proved to be the most difficult one to deposit by electron beam evaporation. It was difficult to maintain a constant rate of evaporation for the required length of time. As a result, we investigated the possibility of evaporating tungsten trioxide from a ribbon of the metal.

A tungsten ribbon of dimensions .003" x 3/8" x 5" is clamped between two current leads from a step-down current transformer. The strip is oxidized in air by passing a large current through it. By observing the colors on the ribbon, the resulting oxide thickness can be controlled and is highly reproducible. The system is then evacuated and the oxide flashed off and deposited on the wafers by resistance heating the strip.

DOPANT DEPOSITION BY SPUTTERING

Sputtering was carried out in a vacuum system filled with argon to a pressure of $1.8 \cdot 10^{-2}$ torr., after having been previously evacuated to 10^{-6} torr. Sputtering targets were 6 in. in diameter, and the distance between targets and substrates was 1.5 inches. A sputtering power of 50 watts was used. This resulted in a deposition rate of 6 A/min. Only Cr and Ni were sputtered.

DOPANT DEPOSITION BY SOLUTION DOPING

Very dilute solutions (0.00018M) of Cr or Ni were prepared. From 1 to 3 cm^3 of solution were then metered out and the solvent evaporated on the wafer surface. The resulting dopant concentration was not uniform over the wafer, however, the dopant concentration being higher at the wafer edges due to the accumulation of solute at the edges where the solvent evaporated last.

ANALYTICAL PROCEDURES

When the dopant was evaporated, the deposited dopant concentration was monitored by the frequency change of a 4 MHz quartz crystal. The quartz crystal, in turn, was calibrated in blank runs in which metal was deposited on an oxidized Si wafer to a coverage of about 100 monolayers, which was accurately determined by atomic absorption measurements. This was then compared to the corresponding frequency change. The sensitivity of the quartz crystal used was .0078 microgram/Hz.

When the dopant was sputtered, the dopant concentrations were determined from the sputtering time at a sputtering voltage and current for which the sputtering rate has been previously determined in blank experiments using dopant thicknesses of 500 to 1000 A.

In experiments involving solution doping, very dilute (0.00018M) solutions of the dopants (Cr and Ni only) were prepared. From 1 to 3 cm^3 of solution were then metered out and the solvent evaporated on the wafer surface. The average dopant concentration was then calculated from the quantity of solute contained in the solution, which was known to three significant figures.

Auger analysis of the wafer surface after dopant deposition clearly shows the presence of the dopant. This is illustrated in Fig. 6 for tungsten. In addition to the expected elements, a strong carbon peak is always visible, probably due to the long storage time before analysis. The Auger peak-to-peak distance for the various W lines obtained for a number of W concentrations corresponds reasonably well to the surface concentration calculated from the quartz crystal frequency change. This is illustrated in Fig. 7 for tungsten as the dopant, for the tungsten lines corresponding to 160 and 1700 ev Auger electron energy.

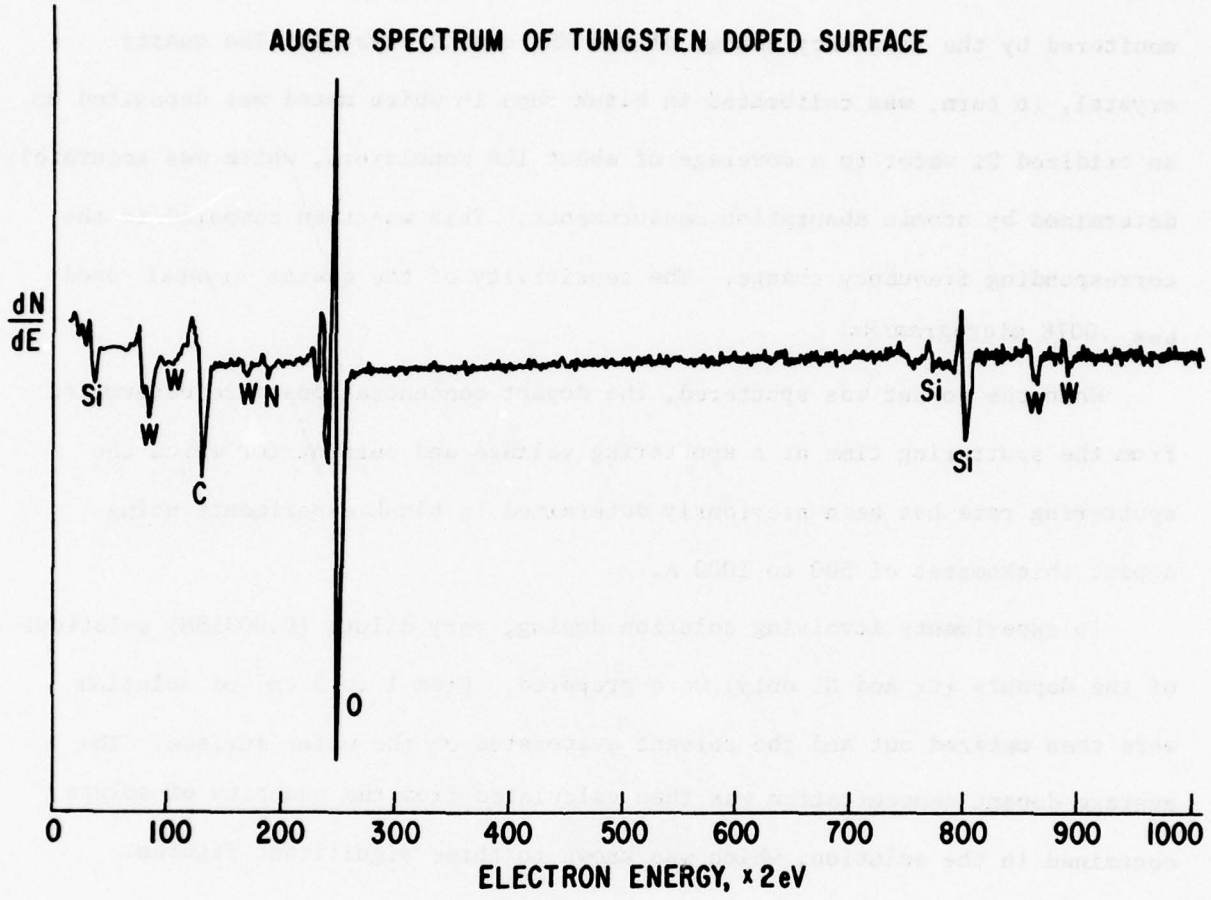


Figure 6. Auger Spectrum of Tungsten Doped Surface

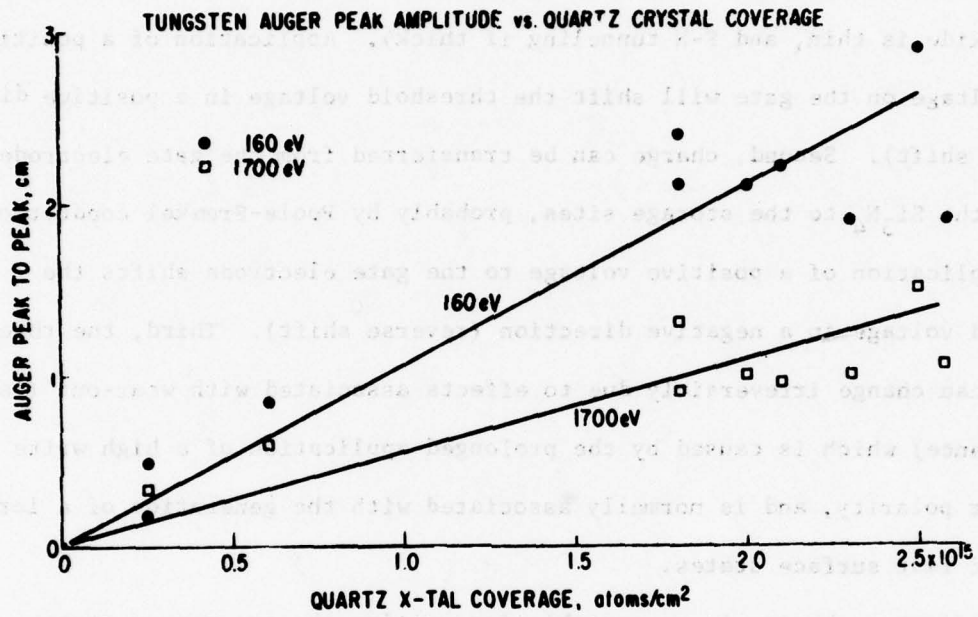


Figure 7. Tungsten Auger Peak Amplitude vs. Quartz Crystal Coverage

SECTION V

WRITE CHARACTERISTICS

WRITE MECHANISMS AND WRITE CURVES

The three mechanisms by which the threshold voltage in interface doped MNOS devices can be changed are illustrated in Figure 8. First, charge can be transferred through the thin oxide by a tunneling process (direct tunneling if the oxide is thin, and F-N tunneling if thick). Application of a positive write voltage on the gate will shift the threshold voltage in a positive direction (forward shift). Second, charge can be transferred from the gate electrode through the Si_3N_4 to the storage sites, probably by Poole-Frenkel conduction. Here, application of a positive voltage to the gate electrode shifts the threshold voltage in a negative direction (reverse shift). Third, the threshold voltage can change irreversibly due to effects associated with wear-out (lack of endurance) which is caused by the prolonged application of a high write voltage of either polarity, and is normally associated with the generation of a large number of fast surface states.

The first mechanism is responsible for writing the two memory states. It is essentially temperature independent. The second mechanism, which is strongly temperature dependent, has not been found to be the predominant one in this investigation. Note, however, that Thornber[2] et al have reported that the second mechanism is important in determining retention.

To write, a sufficiently high write voltage must be applied for a sufficient length of time. The lower the write voltage, the longer the time required to transfer the charge to the storage sites and change the threshold voltage. This is schematically indicated in Fig. 9, where the expected threshold voltage shift is shown as a function of the write pulse width for various write pulse amplitudes (full lines). The expected behavior is shown for initial memory

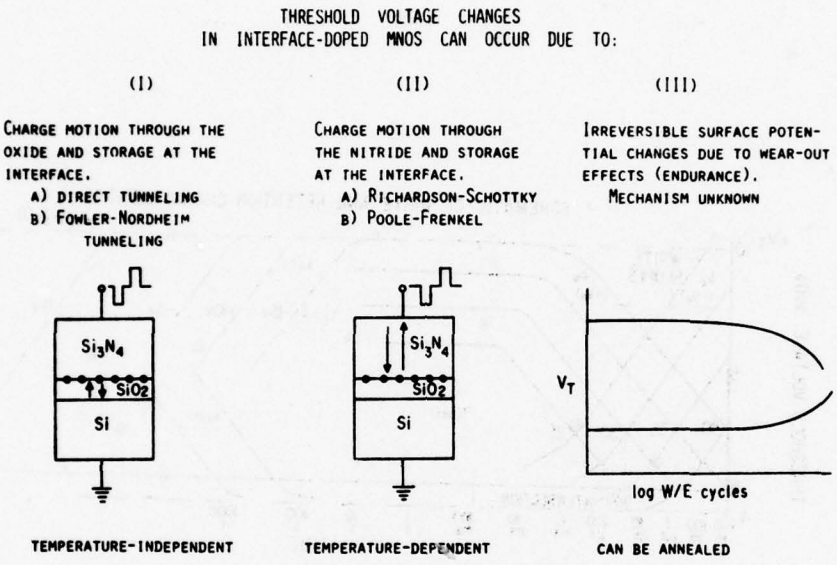


Figure 8. Threshold Voltage Changes in Interface-Doped MNOS

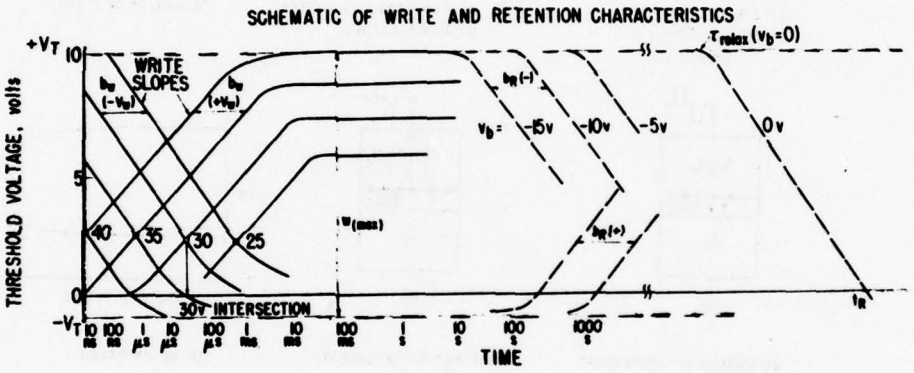


Figure 9. Schematic of Write Characteristics

states for which the threshold voltage is -1 V and also + 10 V, and to which a positive and negative write voltage is applied, respectively. When the write voltage is first applied, the threshold voltage changes rapidly due to the high field across the thin oxide. However, the threshold voltage must be expected to saturate soon as more and more charge is stored at the dopant sites and the field is reduced. The time at which the threshold voltage levels out with time depends on the write pulse amplitude.

The write curves for negative applied write voltages are roughly mirror images of those for positive applied voltage. The point at which the curves for a particular write voltage $-V_w$ and $+V_w$ intersect is an indication of the speed with which the device can be written. We have taken the time associated with the intersection of the 30 V write curves to characterize the device write speed. At the pulse width corresponding to the 30 V intersection, about half of the saturation memory window is written for a 30 V pulse amplitude.

It is found experimentally that the spacings b_w on the log time axis, between write characteristic curves expressed in decades of write time per volt of write voltage are approximately equal in the range of voltages from 20 to 40 V, which were normally used for writing. Also, the slopes of the write curves, expressed in volts of threshold voltage change per decade of applied write pulse time, are approximately equal for all write voltages of the same polarity. The same is true for both polarities, except that the sign of the slopes are changed.

WRITE CHARACTERISTICS OF P-CHANNEL DEVICES

The schematic behavior indicated in Fig. 9 is actually followed quite well for p-channel devices, as indicated in Fig. 10 where actual experimental write curves are plotted for a chromium interface doped p-channel varactor for write voltages of $\pm$ 25V to $\pm$ 40V and pulse widths between 5μs and 10s.

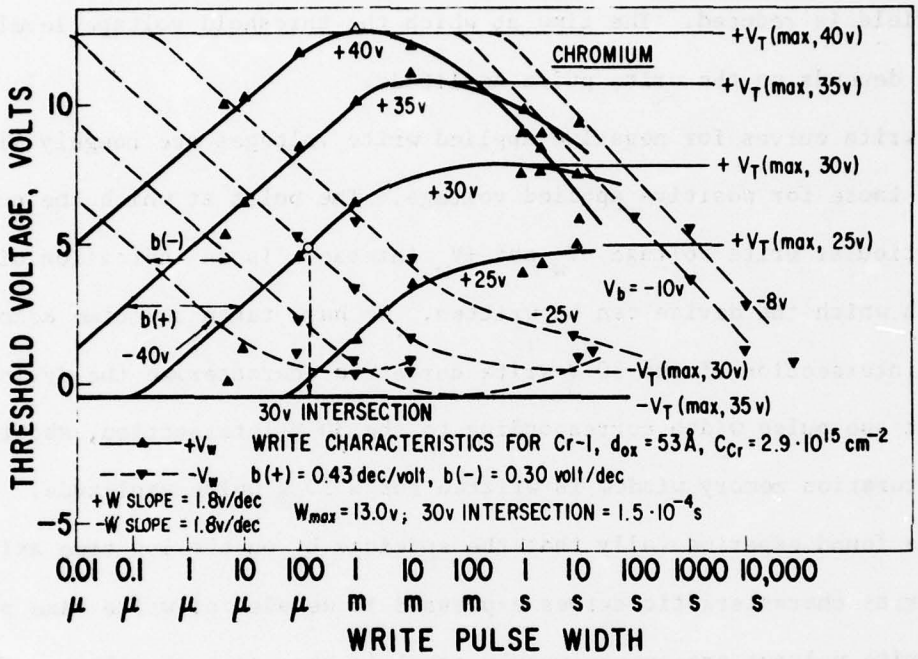


Figure 10. Write Characteristics of Chromium Doped p-channel Varactors

The write behavior of this device can be characterized by a write slope of 1.8 V/dec, a spacing b_w between write curves of 0.43 dec/volt for positive write voltages and -0.30 dec/volt for negative write voltages, and a "30 V intersection" of 100 μs, meaning that approximately a 5V window can be written at a 100 μs write pulse width and a 30V write pulse amplitude.

It can also be seen from Fig. 10 that the threshold voltage does not saturate with pulse width, as predicted by Fig. 9, but goes through a maximum and then decreases again. This is particularly true for write voltages in excess of 25 V. For example, after a 100 sec write pulse, the threshold voltage window characterizing the two memory states is smaller at V_W = 40 V than it is at 30 V,and the window may, in fact, close down completely for very long write times. Devices which have been written past the maximum threshold window have sustained at least some permanent wear-out damage and cannot be fully re-written. They act instead like devices which have been cycled beyond their endurance limit. This effect is always associated with an increase in the surface state density. We have taken the maximum memory window achievable for any write pulse width or amplitude (up to 40V) as the "saturation memory window." The saturation memory window of the device in Fig. 10, for instance, is from +12.5 to -0.5, for a maximum window of 13 V, at $V_w = \pm 40$ V.

Comparison with undoped devices

It is in the write characteristics where the beneficial role of interface doping can be demonstrated best. Figure 11 illustrates the write characteristic curves of two devices which differed from each other only in that one was doped with $1.1 \cdot 10^{15}$ cm^{-2} of Pt, and the other was undoped. (They were adjacent on the same wafer.) Writing with both polarities gives the curves shown in Fig. 11, starting from the opposite saturated memory state. It can be seen that the write curves are essentially identical for the doped

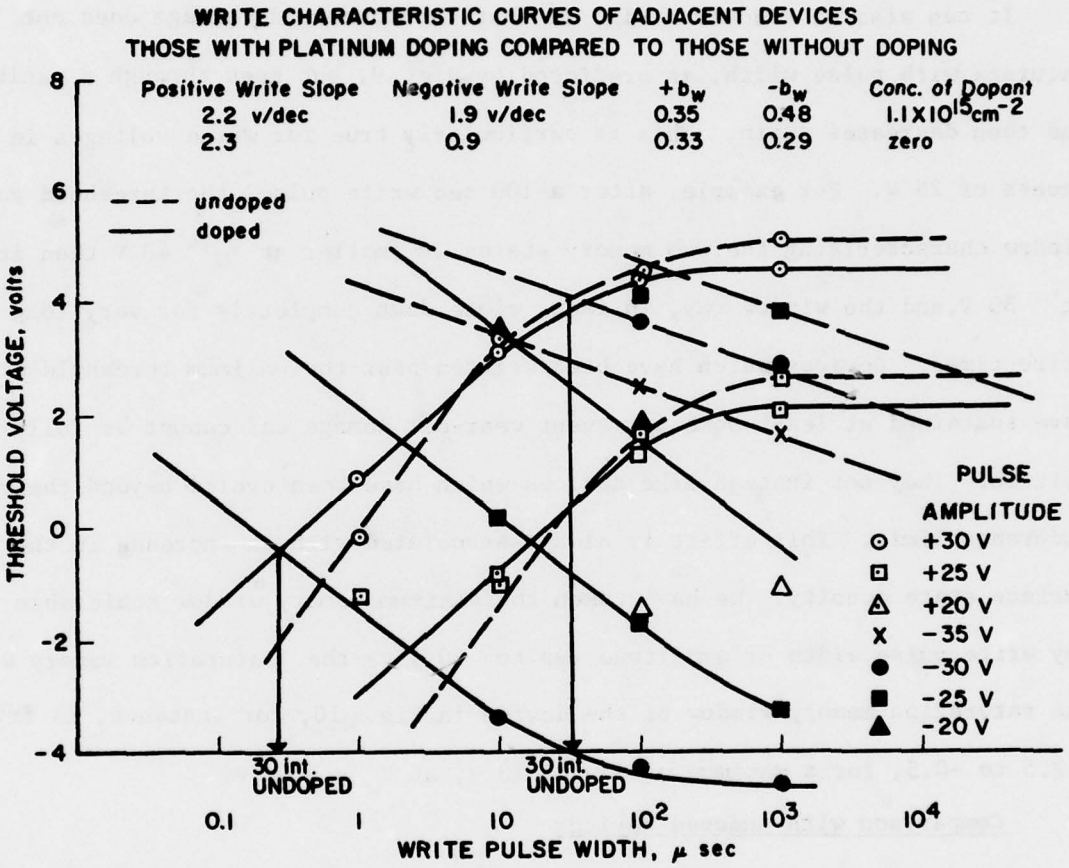


Figure 11. Write Characteristic Curves of Doped and Undoped p-channel Devices

and undoped devices when the write voltage is positive. However, for negative write voltages, the undoped device needed much longer pulse widths to bring about the same threshold voltage change which was obtained for much shorter pulse widths in the doped device. Thus, a 1 ms pulse at -35V gives the same threshold voltage change for the undoped device as a 0.1 ms pulse at -20V for the doped device.

The differences in the write characteristics between a doped and undoped device can be summarized as follows:

a) The undoped device cannot eject negative stored charge from the interface back to the silicon as quickly as the doped device.

b) The negative write slope for the undoped device is only half that of the doped devices.

c) The spacing between negative write curves, $-b_w$, for the undoped device is only half that for the doped device.

Dependence of write speed on dopant concentration

It was generally found that the write speed increased with increasing dopant concentration. This dependence is not strong, however, and is easily clouded by even small differences in oxide and nitride thicknesses. In addition, if the dopant diffused deeper into the oxide, due to exposure to a longer or higher temperature wafer processing cycle after deposition, then high write speeds can be observed even at relatively low concentrations.

Figure 12 shows the normally observed behavior. Here the 25 volt intersection is plotted as a function of the chromium dopant concentration for a set of increasing oxide/nitride thicknesses. The write speed increases by about two orders of magnitude for an increase in the doping by one order of magnitude.

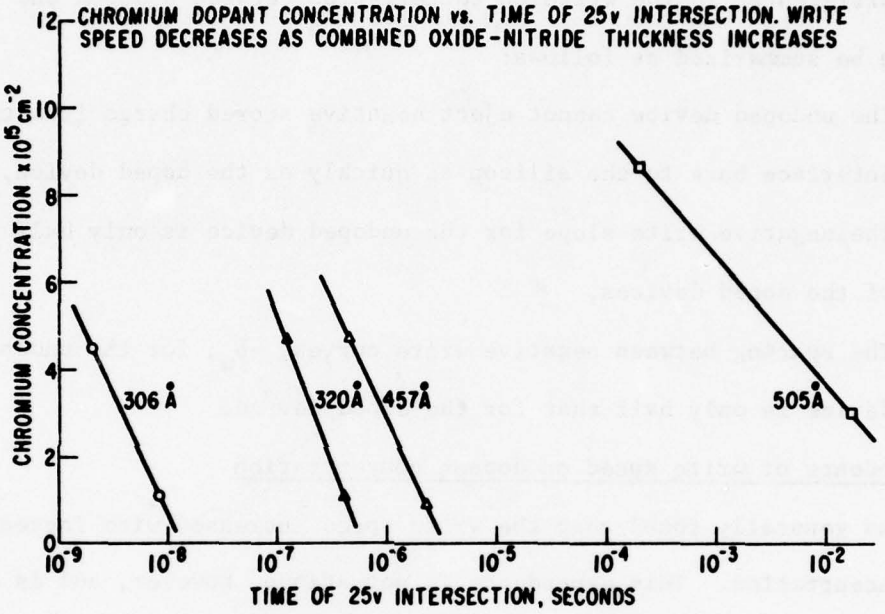


Figure 12. Cr Dopant Concentration vs. Time of 25V Intersection for p-channel Devices

Dependence of write speed on oxide thickness

The oxide thickness has a strong influence on write speed. Although this influence is again clouded somewhat by the varying degrees of diffusion of the dopant in the oxide, the dependence of write speed on oxide thickness is generally as shown in Fig. 13, which displays the dependence for fast-write devices. An increase in the oxide thickness of 20A decreases the write speed by about 3 orders of magnitude.

Temperature dependence

The temperature dependence of the write characteristics is small. This is to be expected if writing occurs by charge transfer through the oxide by F-N tunneling which is, to a first order approximation, temperature independent. This is illustrated in Fig. 14, which shows the +25 V write characteristic curve for platinum doped varactors at various temperatures between 25°C and 300°C. At 300°C, the second write mechanism discussed above is perhaps coming into play, reducing the effective charge transferred by F-N tunneling, and thus resulting in a small threshold voltage shift. The principal conclusion is, therefore, that the write mechanism is by F-N tunneling at least up to 250°C.

WRITE CHARACTERISTICS OF N-CHANNEL DEVICES

The write behavior of n-channel devices was quite analogous to that for p-channel devices in all respects, except that the memory window is predominantly in the non-conducting region of the transistor. This makes the n-channel device more desirable for circuit applications.

This is illustrated in Fig. 15 and Fig. 16 for a W-doped and Pt-doped n-channel varactor, respectively. Here the experimental write curves are plotted for write voltages of $\pm$20V to $\pm$30V and pulse widths between 1 μs and 10 ms. The write behavior of these devices can be characterized by write

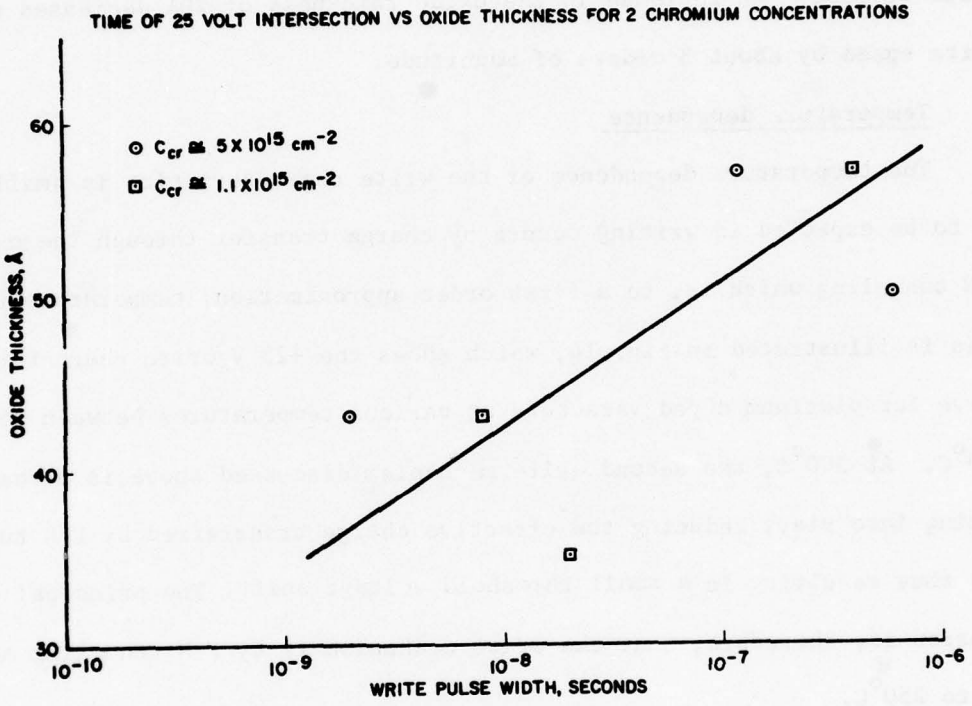


Figure 13. Time of 25V Intersection vs. Oxide Thickness

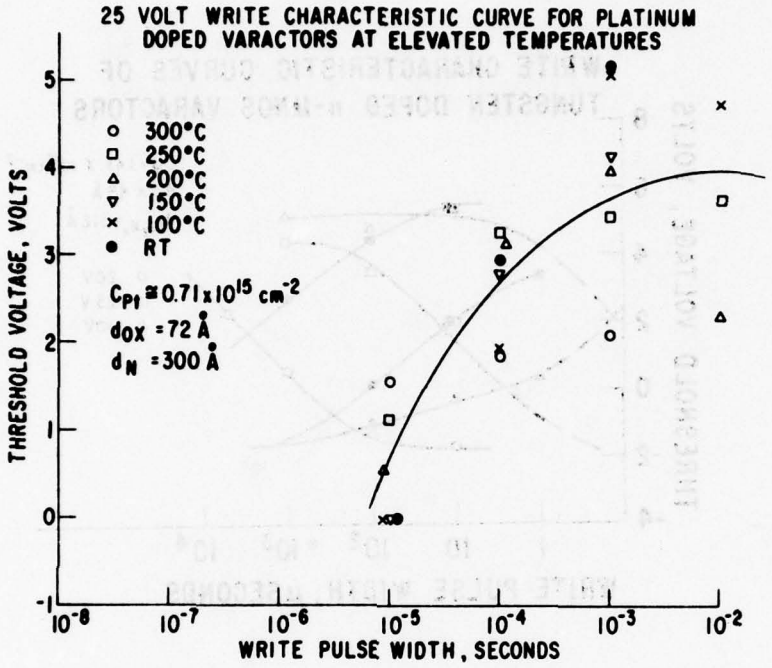


Figure 14. 25V Write Characteristic Curve at Elevated Temperatures

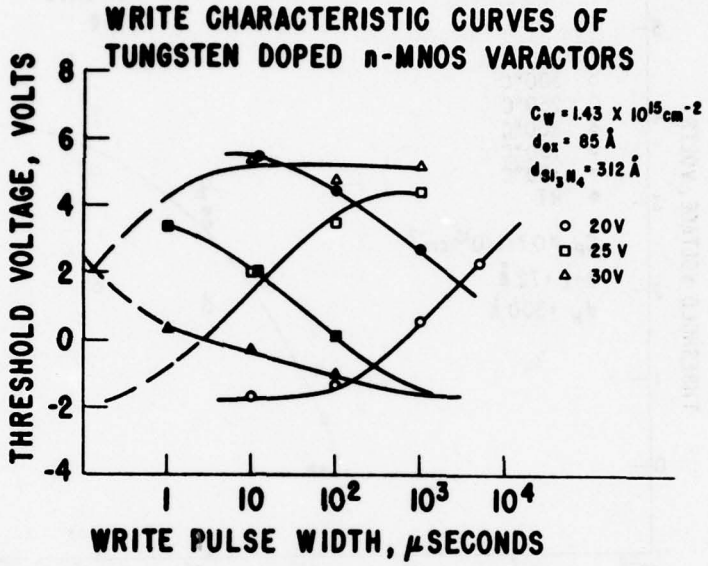


Figure 15. Write Characteristics of Tungsten Doped N-Channel Varactors

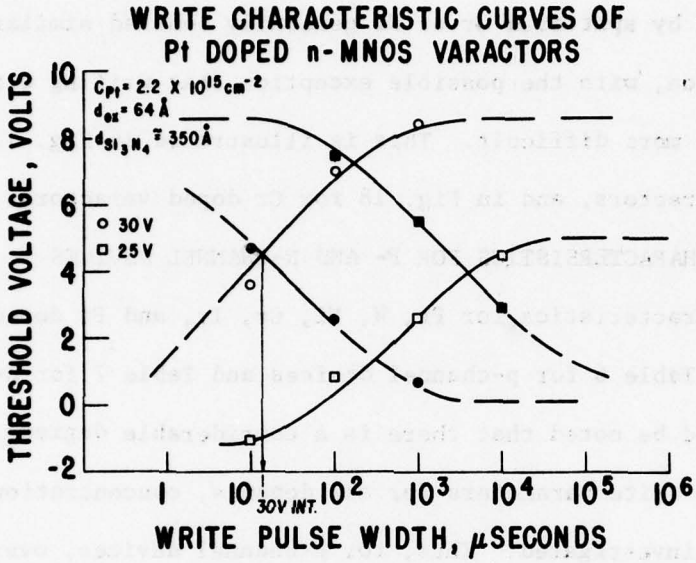


Figure 16. Write Characteristics of Platinum Doped N-Channel Varactors

slopes, b_w spacings, and 30V intersections, just as the p-channel devices described above (see Tables 6 and 7). In particular, the 30V intersection is at only a few microseconds, indicating fast write devices for that voltage. Conversely, these devices can be written more slowly, namely in about 10 ms, by using write voltages as low as 20V.

WRITE CHARACTERISTICS OF DEVICES DOPED BY SPUTTERING

Devices doped by sputtered Cr or Ni generally behaved similarly to those doped by evaporation, with the possible exception that writing with negative write voltages was more difficult. This is illustrated in Fig. 17 for Ni doped p-channel varactors, and in Fig. 18 for Cr doped varactors.

SUMMARY OF WRITE CHARACTERSISTICS FOR P- AND N-CHANNEL DEVICES

The write characteristics for Pt, W, Ni, Cr, Ir, and Pt doped devices are summarized in Table 6 for p-channel devices and Table 7 for n-channel devices. It should be noted that there is a considerable degrees of similarity between the write parameters for all dopants, concentrations, and oxide thicknesses investigated. Thus, for p-channel devices, over the entire dopant concentration (10^{14} to 10^{16} cm^{-2}) and oxide thickness range (40 to 140A) studied, and all of the dopants investigated, the write slope was always 2.0 ± 0.5 V/dec, and the spacing b_w was 0.40 ± 0.10 dec/volt with only minor exceptions. The saturation (maximum) memory window was generally around 10V. Similarly, for n-channel devices, the write slope was always 3.0 ± 0.5 V/dec, and the spacing b_w was 0.50 ± 0.10 dec/volt, again with only minor exceptions. The saturation memory window was around 10V for n-channel devices, also.

The parameter which does differ the most between devices is the "30 V intersection." The shortest "30 V intersections" are obtained for the thinnest oxide films and the highest dopant concentrations. For p-channel

TABLE 6

WRITE PARAMETERS FOR P-CHANNEL MEMORY DEVICES

Dopant	Var. or Transistor	Dopant conc. $\times 10^{15}$ cm^{-2}	d_{ox}, A	d_{Nit}, A	Write slope V/dec $+V_w$	b_w, dec/volt $+V_w$	$+V_{T,max}$ volts	W_{max}, volts	30 volt intersect. sec.	Fast Write
Chromium	V	2.95	53	452	1.80	0.43	12.5	13.0	1.5×10^{-4}	
	V	2.95	134	452	1.80	0.43	8.8	9.1	1.1×10^{-4}	
	V	8.6	53	452	1.70	0.43	10.4	10.7	1.8×10^{-6}	
	V	8.6	134	452	1.80	0.27	5.9	6.3	4.0×10^{-4}	
	V	1.32	88	372	1.80	0.31	10.5		3.1×10^{-4}	
	T	1.59	85	372	1.80	0.31	5.0	6.4	3.2×10^{-6}	
	T	1.1	43	263	1.45	0.43	3.8	5.8	8.0×10^{-9}*	F
	T	1.1	35	263	1.62	0.36	3.9	5.8	2.0×10^{-8}*	F
	T	1.1	57	263	1.72	0.53	> 4.1	> 6.4	4.0×10^{-7}*	F
	T	4.5	43	"	1.65	0.35	4.1	6.0	2.0×10^{-9}*	F
	T	5.4	50	"	2.55	0.36	5.4	8.6	3.5×10^{-7}*	F
	T	4.7	57	"	2.0	0.37	4.6	6.7	1.2×10^{-7}*	F
	T	1.59	85	372	1.8	0.31	5.0	6.4	3.2×10^{-6}	
	T	0.81	"	"	1.5	0.38	4.1	5.8	7×10^{-8}	
	T	3.9	"	"	1.48	0.36	5.4	7.1	1.4×10^{-8}	
Platinum	V	0.51	70	452	1.95	0.37	8.0	11.0	4.0×10^{-5}	
	V	0.42	113	452	1.95	0.35	8.5	11.5	8.0×10^{-4}	
	V	2.28	70	452	1.95	0.41	10.0	13.0	5.6×10^{-5}	
	V	2.10	134	452	1.95	0.34	9.6	12.1	4.0×10^{-3}	
	V	0.40	88	372	1.80	0.32	8.0	11.0	4.0×10^{-5}	
	T	0.27	85	372	1.3	0.48	3.2	5.4	2.5×10^{-6}	
	T	0	85	372	2.27	0.33	5.2	3.6	3.5×10^{-5}	
	T	1.1	85	372	2.2	0.35	4.6	9.2	2.5×10^{-7}	
	T	0.98	85	372	1.8	0.32	5.0	6.2	2.0×10^{-5}	
	T	0.12	58	320	1.3	0.48	4.4		1.5×10^{-7}*	F
Iridium	V	0.081	53	468	2.6	0.33	9.0	9.6	4.5×10^{-4}	
	V	0.081	80	"	2.3	0.44	9.0	9.3	1.8×10^{-3}	
	V	1.09	80	"	2.1	0.50	9.0	14.0	1.1×10^{-3}	
	V	0.49	53	"	2.2	0.30	6.8	7.8	1.0×10^{-5}	
	V	0.21	58	320	1.6	0.48	6.2		4.0×10^{-7}	F
Tungsten		0.60	85	372	2.2	0.32	5.5	6.7	2.0×10^{-5}	
	V	0.55	63	450	1.3	0.43	8.0	9.0	8.0×10^{-2}	
	V	2.52	63	"	1.25	0.45	7.0	7.5	1.0×10^{-1}	
	V	2.52	94	"	1.0	0.41	6.5	7.3	2.0×10^{-1}	
	V	0.363	85	468	2.8	0.32	8.8	9.8	2.0×10^{-4}	
	V	0.363	53	"	2.7	0.36	8.8	9.1	3.0×10^{-5}	
WO_3	T	1.79	84	280	1.12	0.40	4.6	9.5	6.0×10^{-7}	
WO_3	V	1.94	58	320	0.9	0.92	7.7		2.0×10^{-9}	F
Palladium	V	0.47	70	452	1.93	0.32	7.5	9.5	1.0×10^{-3}	
	V	0.47	134	452	1.93	0.34	5.5	7.5	4.0×10^{-3}	
	V	4.2	70	452	1.93	0.40	7.0	7.0	4.0×10^{-5}	
	V	4.2	134	452	1.75	0.33	4.0	4.0	1.0×10^{-2}	
	T	0.86	85	372	1.63	0.33	3.3	5.3	1.7×10^{-5}*	F
	T	1.58	85	372	1.6	0.4	2.4	4.3	6.5×10^{-8}	
Nickel	V	0.266	53	468	2.0	0.49	9.5	5.0	10^{-3}	
	V	0.266	85	468	2.6	0.464	8.0	10.0	4.0×10^{-4}	
	V	1.22	53	468	2.5	0.33	9.5	12.0	2.0×10^{-4}	
	V	1.22	85	468	3.4	0.34	7.5	-	10^{-3}	
	V	0.66	58	320	1.8	0.34	6.1		2.0×10^{-8}	F

* Time of 25 V intersection instead of 30V intersection.

TABLE 7

WRITE PARAMETERS FOR N-CHANNEL MEMORY DEVICES

Dopant	Dopant Conc. $\times 10^{15}$ cm^{-2}	d_{ox} Å	d_{Nit} Å	Write slope V/dec $+ V_w$	b_w dec/V $+ V_w$	$+ V_{T,max}$	30 volt intersect. µsec	W_{max}, V
Platinum	3.6	80	~ 350	3.4	.45	8.8	40	9.1
	2.2	"	"	3.1	.36	8	20	9.9
	0.8	"	"	3.2		7.9		9.1
	0.8	64	"	3.2	.35	8.1	2	9.6
	2.2	"	"	3.4	.41	9	8	11.2
	3.6	"	"	2.5	.53	8.3	10	10.3
	0.3	54	"	2.8	.49	8		1.1
	0.7	"	"	3.3	.63	9.4	400	6.4
	1.1	"	"	3.5	.55	7.8	300	6.2
	1.1	80	"	2.8	.56	7	900	5.8
	0.7	"	"	3.4	.57	8.1	300	7
	0.3	"	"	4.1	.41	8.1	60	4.6
	0.3	64	"	3.5	.36	8.5	200	3.6
	0.7	"	"	2.7	.39	9.8	500	7.8
	1.1	"	"	2.6	.53	8.2	500	7
	2.7	85	312			6.6	1.1	9.2*
Iridium	0.3	54	~ 350	3	.39	10	150	2.8
	0.7	"	"	2.6	.52	10.4	480	5
	1.1	"	"	3.6	.48	10.2	400	6
	0.3	64	"	2.1	.52	9.4	80	3.4
	0.7	"	"	3	.48	9.4	410	5
	1.1	80	"	3	.49	6.6	130	4.6
	0.7	"	"	3.4	.47	8.8	800	4.8
	0.3	"	"	2.6	.54	8.6	70	5.2
Tungsten	1.4	85	312	1.7	.55	5.9	10	7.6
Chromium	4.1	85	312	2.2	.41	6.4	.6*	8
	1.0	54	~ 350	2.8	.49	8.2	800	1.7
	1.7	54	"	2.7	.51	8.9	100	5.3
	1.0	64	"	3.0	.51	8.3	70	3.3
	1.7	64	"	2.2	.53	8.5	40	6.1
	1.7	80	"	2.7	.38	7.4	100	4.4

* 25V int.

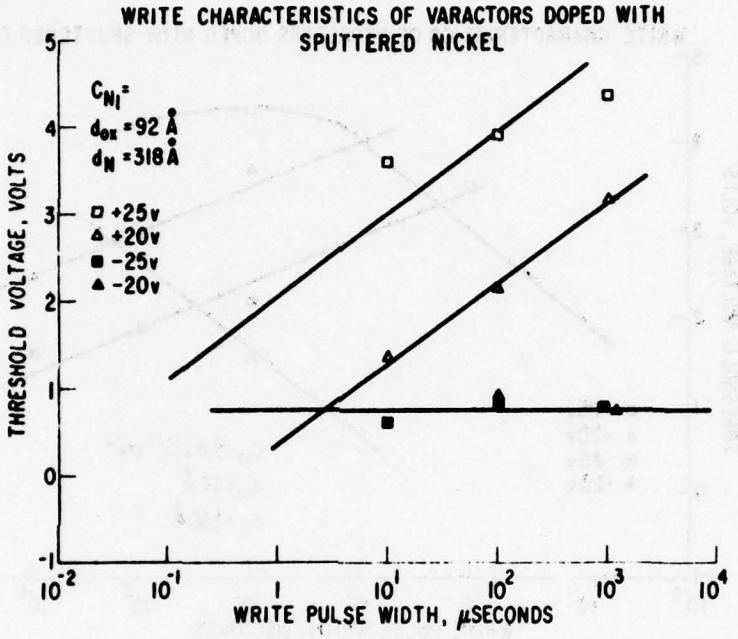


Figure 17. Write Characteristics of p-channel Varactors Doped with Sputtered Nickel

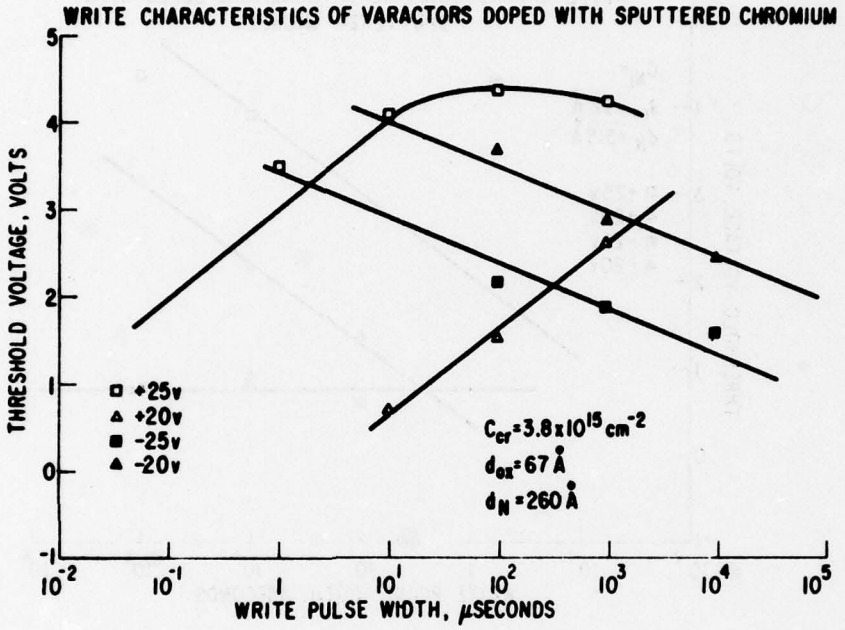


Figure 18. Write Characteristics of p-channel Varactors Doped with Sputtered Chromium

devices, the lowest value is $2 \cdot 10^{-9}$ sec, obtained for a 48 A oxide film and a Cr dopant level of $4.5 \cdot 10^{15}$ cm^{-2}, and a 58 A oxide film and a WO_3 concentration of $1.94 \cdot 10^{15}$ cm^{-2}. For n-channel devices, the lowest value is 2 μs, obtained for a 64A oxide film and a platinum dopant concentration of 0.8 x 10^{15} cm^{-2}. For the thicker oxide films and lower dopant concentrations, values as long as 100 msec have been obtained.

From Tables 6 and 7, it can be concluded that n-channel memory devices increase their memory window more rapidly with time as the write pulse width is increased, which is desirable. On the other hand, as the write voltage is increased, the window in n-channel devices increases less rapidly than for p-channel devices, for the same write pulse width. Overall, the two types of devices are quite comparable in their write characteristics.

SECTION VI

DOPANT CONCENTRATION DEPENDENCE OF MEMORY WINDOW

Dopants were selected in accordance to their reactivity with oxygen. One metal, Ti, has an oxide more stable than SiO_2. Nb and Ta have oxides which are not reducible by hydrogen, while Cr, Mo, W, and Ni have oxides which are reducible by hydrogen. Three metals were chosen for their inertness toward oxidation: Pd, Ir, and Pt.

We have investigated the saturation memory window for 10 different dopants, namely, Pt, W, Ni, Cr, Ir, Pd, Nb, Ta, Mo, and Ti at various dopant surface concentrations between 10^{14} to 10^{16} cm^{-2} and in the oxide thickness range from 40 to 140 A. Reasonably large saturation memory windows were obtained in this range for six dopants: Pt, W, Ni, Cr, Ir and Pd.

The behavior displayed by Pt in Fig. 19 is somewhat typical for these six dopants. The saturation memory window is located principally at positive threshold voltages. The window tends to become smaller at dopant concentrations lower than 10^{14} cm^{-2}, and in some cases, but not always, a closing trend is observed beyond 10^{15} cm^{-2}. It should be noted that the oxide thickness has relatively little effect on the saturation memory window. The write voltage required to achieve the saturation window is higher for the thicker oxide devices, of course, but the maximum achievable window is not.

Behavior similar to Pt was found for W (Fig. 20), Ni (Fig. 21), Cr (Fig. 22), Ir (Fig. 23), and Pd (Fig. 24). An especially detailed picture was obtained for chromium at dopant concentrations between 10^{14} and 10^{15} cm^{-2}. It was found that in this range, somewhat surprisingly, the thinner oxide windows close faster with decreasing dopant concentration than the thicker oxides.

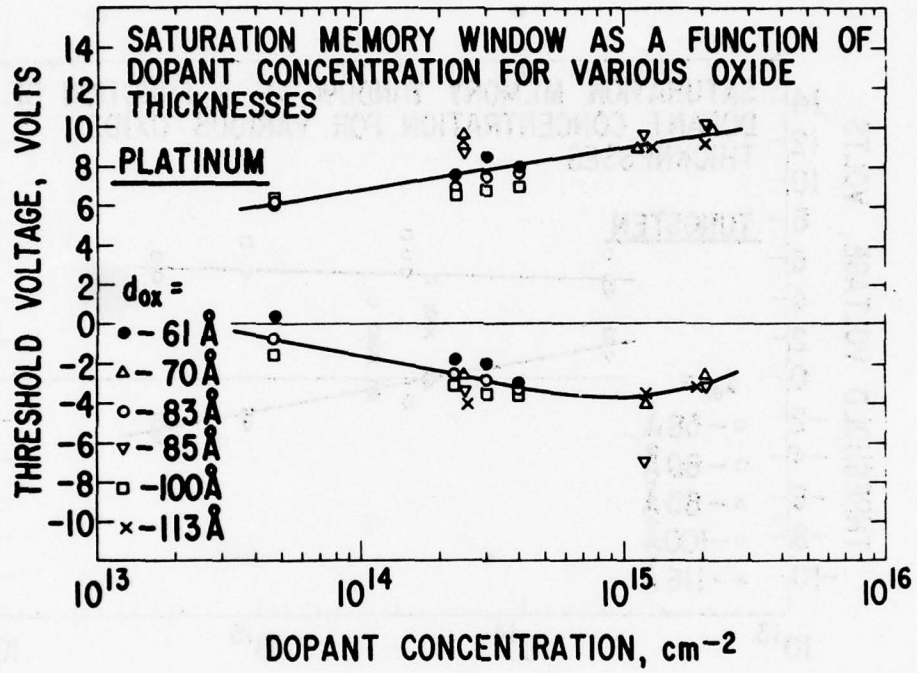


Figure 19. Platinum Saturation Memory Window vs. Dopant Concentration, P-Channel Varactor

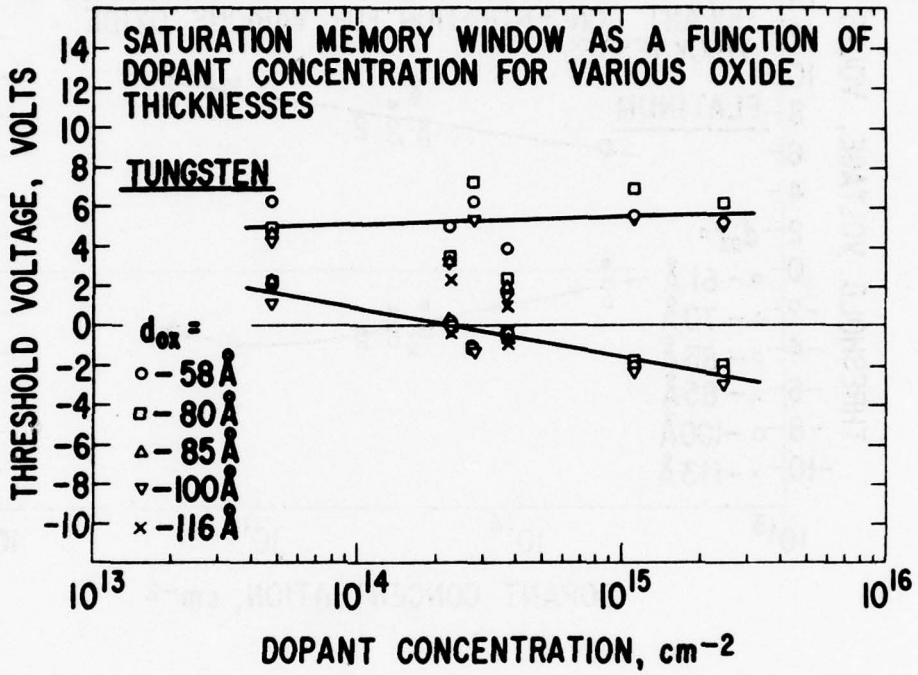


Figure 20. Tungsten Saturation Memory Window vs. Dopant Concentration, P-Channel Varactor

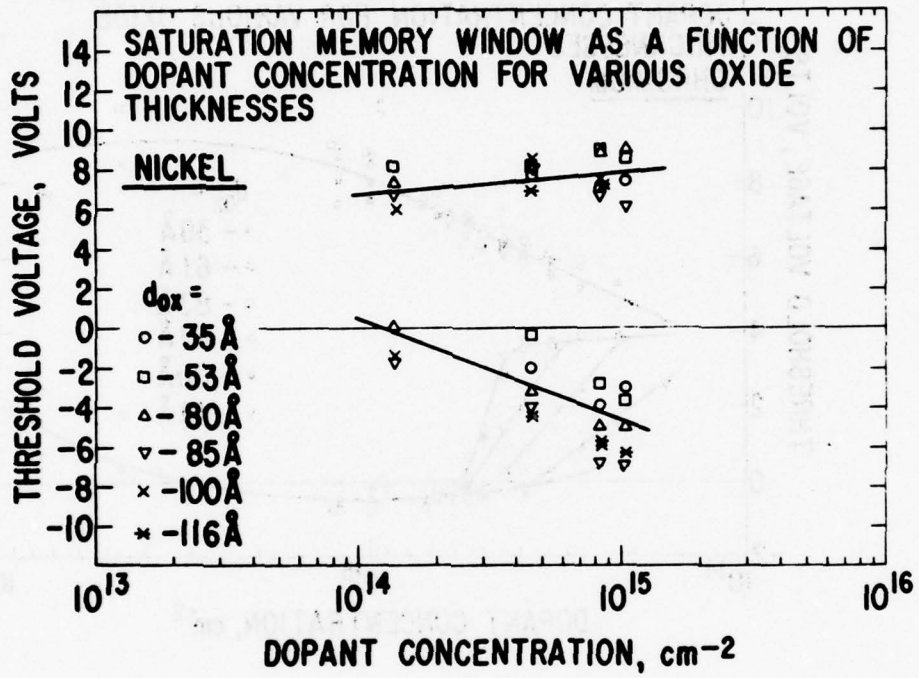


Figure 21. Nickel Saturation Memory Window vs. Dopant Concentration, P-Channel Varactor

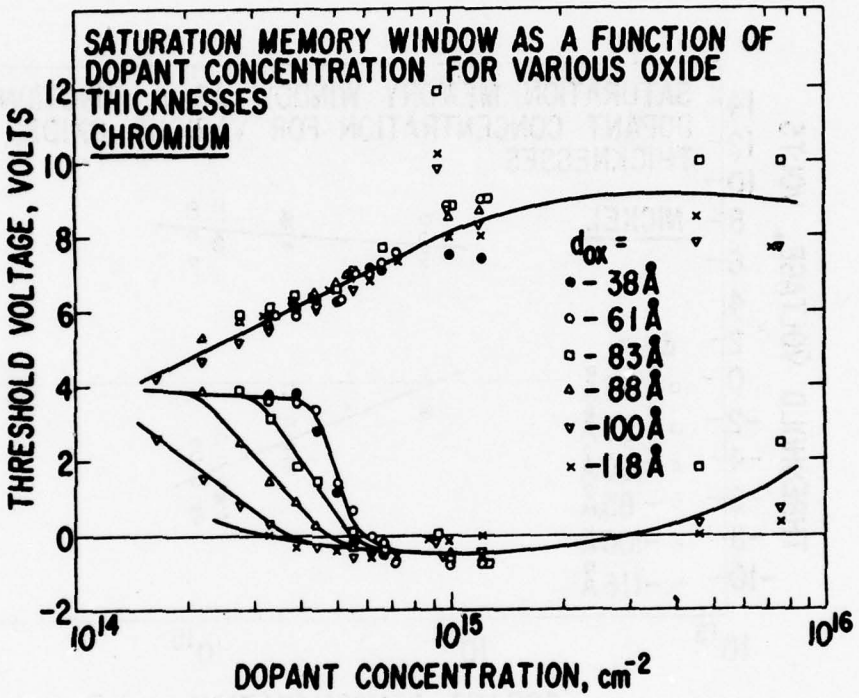


Figure 22. Chromium Saturation Memory Window vs. Dopant Concentration, P-Channel Varactor

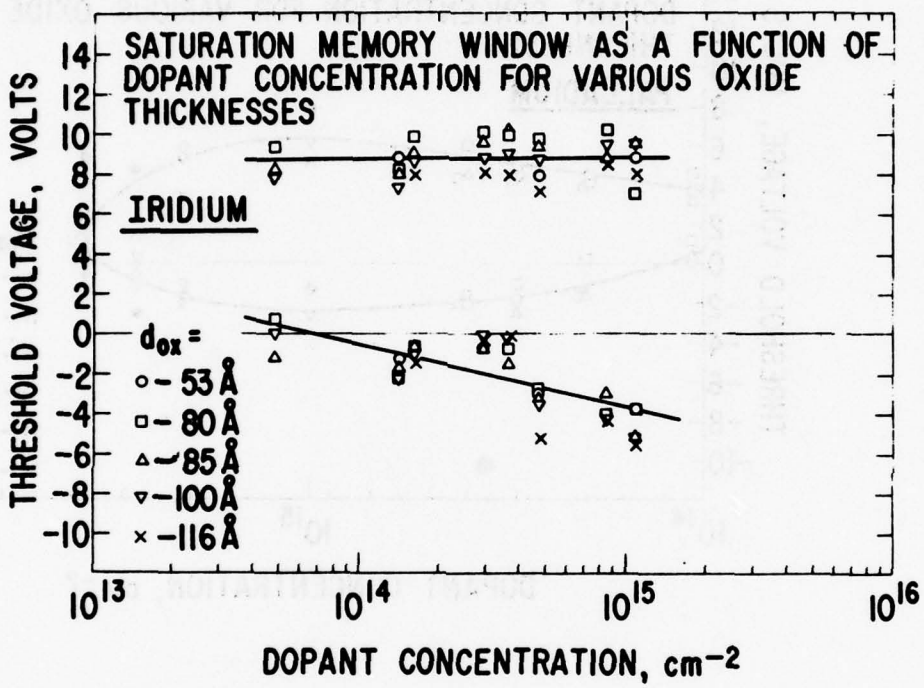


Figure 23. Iridium Saturation Memory Window vs. Dopant Concentration, P-Channel Varactor

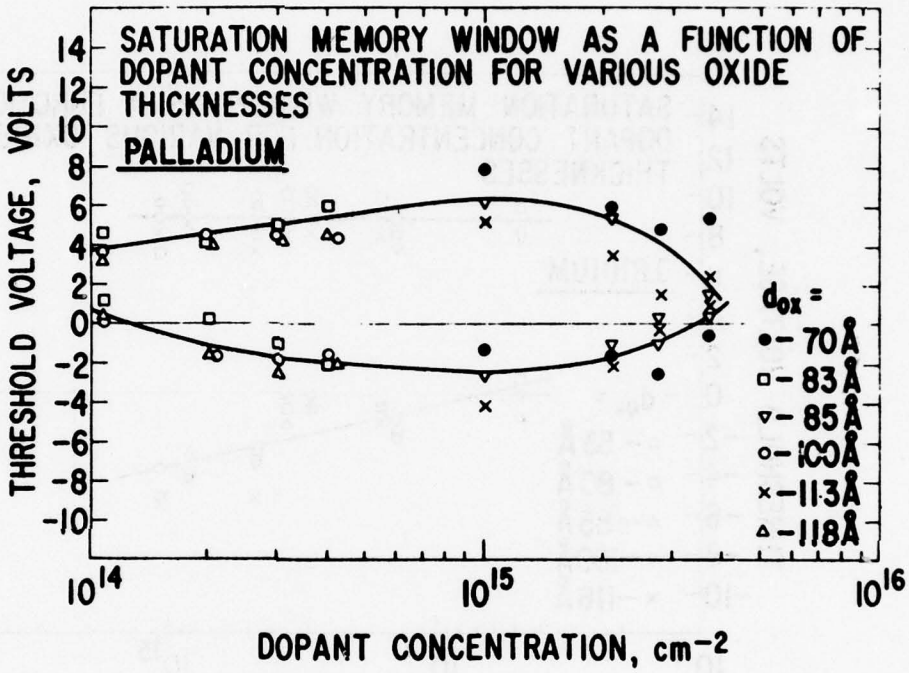


Figure 24. Palladium Saturation Memory Window vs. Dopant Concentration, P-Channel Varactor

These dopants give satisfactory memory windows for applications in arrays. It should be noted that the center voltage of the window indicates that they should be most useful as n-channel devices.

The effect of interface dopant concentration on the memory window for two different oxide thicknesses was also investigated on n-channel varactors. The dopants tested were chromium, platinum, and iridium. The saturation memory window as a function of Ir, Pt and Cr dopant concentrations for n-channel varactors is shown in Figs. 25, 26 and 27, respectively. As was observed for the p-channel devices above, the saturation memory window is located principally at positive threshold voltages. The window tends to become smaller at dopant concentrations lower than 10^{15} cm^{-2}, but a closing trend at higher concentrations has not been observed. The maximum achievable window is independent of the oxide thickness in the range studied.

The use of niobium, tantalum, and molybdenum did not lead to satisfactory results. This is shown in Figs. 28, 29, and 30, respectively, in which the memory window is plotted as a function of dopant concentration for various oxide thicknesses. For niobium and molybdenum, the window was judged to be too small to be useful over the range studied. For tantalum, the additional problem was encountered that, for dopant concentrations above 5x 10^{14} cm^{-2}, Ta diffused through the SiO_2 to the silicon substrate, leading to the disappearance of the memory effect. This was also true for all concentrations of Ti used. It is thus concluded that the more reactive metals are not suitable for memory application.

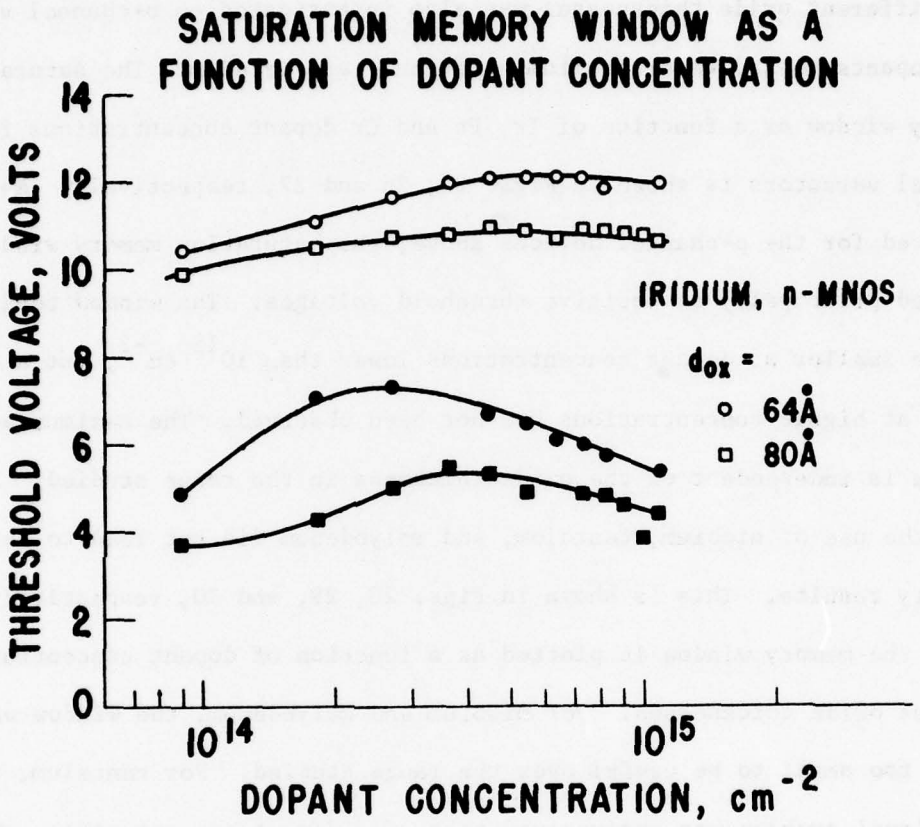


Figure 25. Iridium Saturation Memory Window vs. Dopant Concentration, N-Channel Varactors

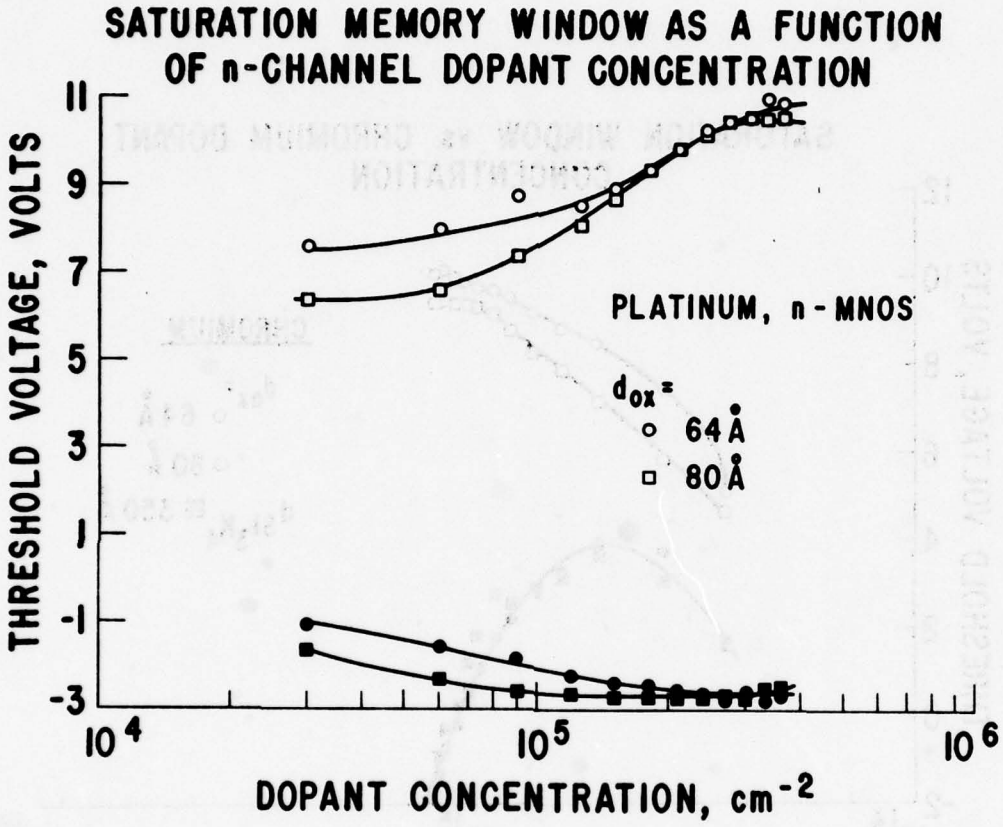


Figure 26. Platinum Saturation Memory Window vs. Dopant Concentration, N-Channel Varactors

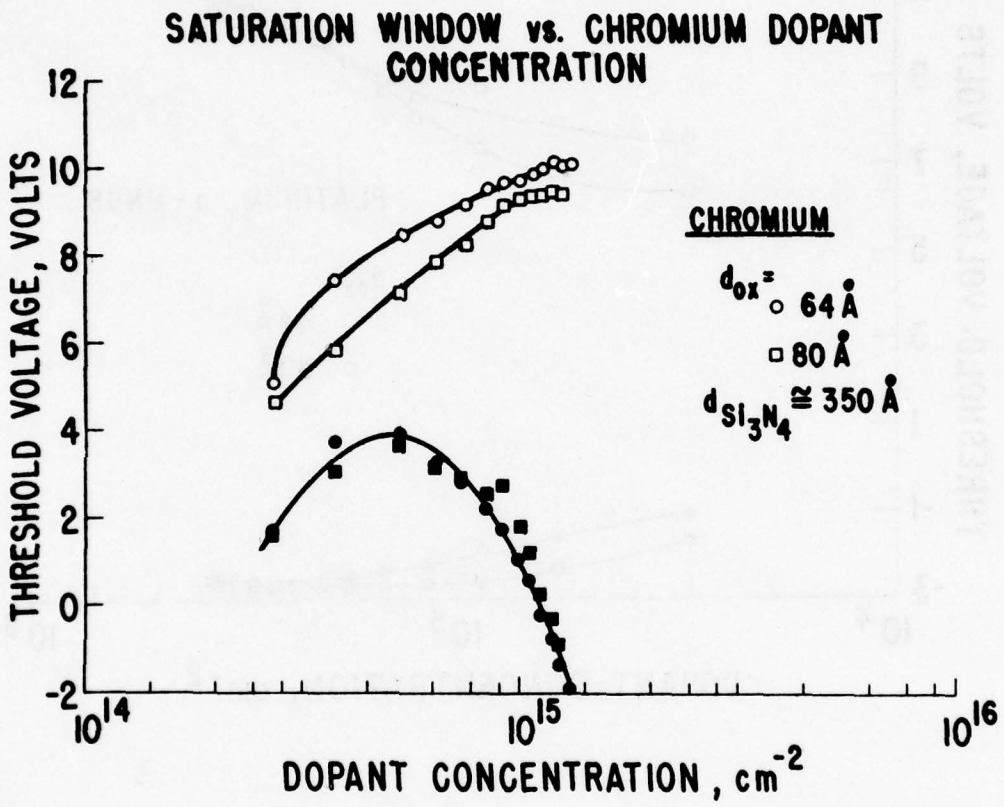


Figure 27. Chromium Saturation Memory Window vs. Dopant Concentration, N-Channel Varactors

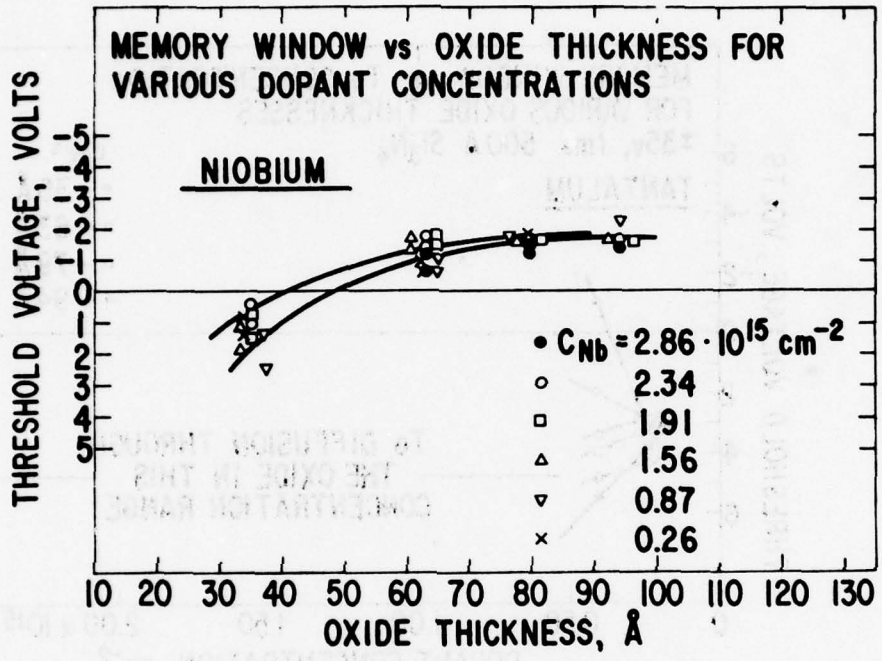


Figure 28. Niobium Memory Windows vs. Oxide Thickness, P-Channel Varactors

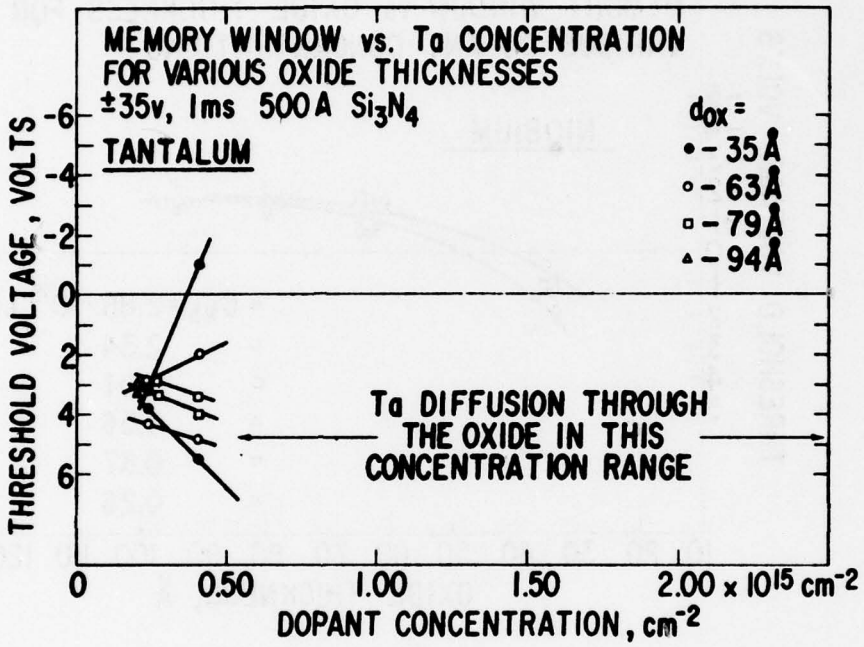


Figure 29. Memory Window vs. Tantalum Concentration, P-Channel Varactors

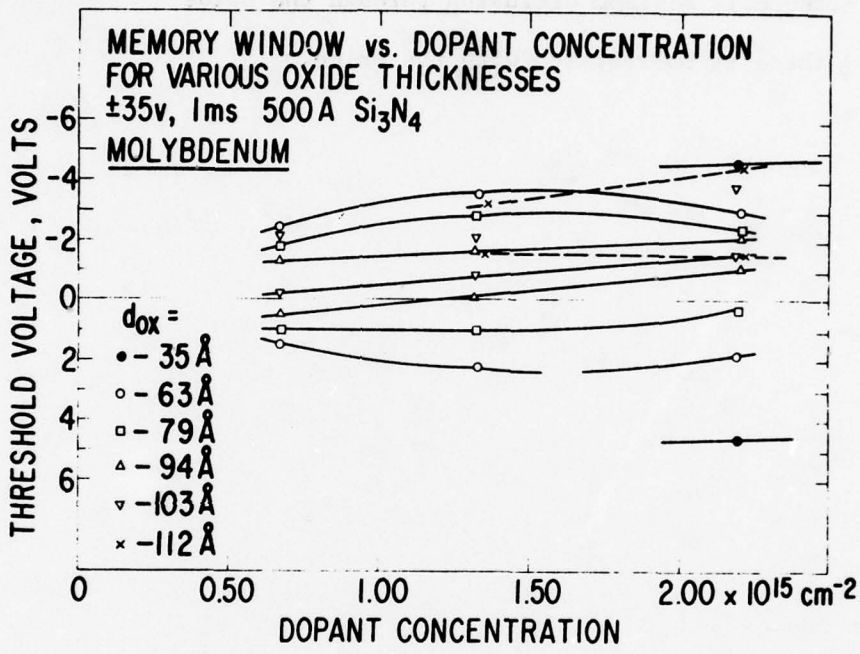


Figure 30. Molybdenum Memory Window vs. Dopant Concentration, P-Channel Varactors

The dopant materials Pt, W, Ni, Cr, Ir and Pd are satisfactory for memory applications because:

- the saturation window is at least 8V
- the saturation window is independent of dopant concentration over at least a decade.
- there is minimum diffusion through the oxide
- there is no reaction with the oxide.

SECTION VII

MEMORY RETENTION

After writing, the charge stored at the dopant sites tends to leak away from the oxide nitride interface in order to decrease the field created by its presence. Charge decay at the dopant sites can occur either by conduction through the memory oxide back to the silicon (writing in the reverse direction) or, by conduction through the silicon nitride to the aluminum.

In the conventional MNOS device, virtually all charge motion occurred through a thin oxide layer via direct tunneling,and charge retention in traps located in the nitride was relatively short. In the case of interface doped MNOS devices, however, the time required for a measurable amount of charge to decay is generally in excess of many months, even years. Fowler-Nordheim back tunneling through the oxide is the dominant mechanism, the oxide is generally thicker, and the dopant traps are deeper.

The high retention of the interface doped devices makes accelerated charge decay tests necessary. Charge leakage through the nitride or oxide, or both, can be accelerated by applying a gate bias voltage to increase the electric field. Conduction through the nitride alone can be accelerated by raising the temperature since it is an activated mechanism.

STORED CHARGE DECAY AS A FUNCTION OF TIME

In general, retention behavior parallels write behavior. It is characterized by a set of curves describing the decay of the threshold voltage as a function of time. The curves are linear on a log time plot over a considerable portion of the memory window. The following parameters are used to describe retention behavior. First there is the decay slope measured in volts/decade, which is analogous to the write slope, and which describes the rate at which the memory states change from one into the other with time for a specific accelerating bias. A second parameter is the spacing between the linear regions

of the characteristic curves, b_R, measured in decades of time per applied bias voltage difference. Thus b_R is quite analogous to b_w, the spacing between the write characteristic curves described earlier. Retention is further characterized by τ_{relax}, the extrapolated charge relaxation time for zero applied bias. The retention time itself, t_R, is the time after writing when memory is finally lost, i.e., the window is closed.

The procedure to estimate τ_{relax}, the time beyond which noticeable charge decay is observed, and also t_R, is as follows. After writing into a device to give a certain threshold voltage shift, normally 6 to 10 volts, an accelerating bias is applied to the gate. The bias is of a polarity opposite that of the writing voltage. In most cases, the retention of the positive threshold voltage state only was studied, since here the negative applied bias voltage adds to the internal field in the oxide due to the electrons stored at the interface. The positive memory state is then the most vulnerable to decay.

Under the applied bias, the threshold voltage decay is recorded as a function of time. When a decay of approximately 5 V has been observed, the measurement is repeated on a similar, neighboring device with a different bias voltage. One such measurement will yield the decay slope, but two are necessary to measure b_R. This procedure is illustrated for a chromium doped p-channel device in Fig. 31. The decay of the threshold voltage was followed for bias voltages of -21,V, -18 V and -16 V. It can be seen that τ_{relax} moves rapidly towards longer times as the bias voltage becomes smaller. Assuming that b_R remains constant down to $V_b = 0$, an extrapolated τ_{relax} ($V_b = 0$) is obtained by displacing τ_{relax} ($V_b = 16$) to the right on the log time scale by the amount $16 \times b_R$. If it is also assumed that the decay slope is the same between 0 and -21 V, t_R can be estimated by drawing a line of the same decay slope from τ_{relax} ($V_b = 0$) to the $V_T = 0$ axis. The time marked by that intersection is taken to be t_R.

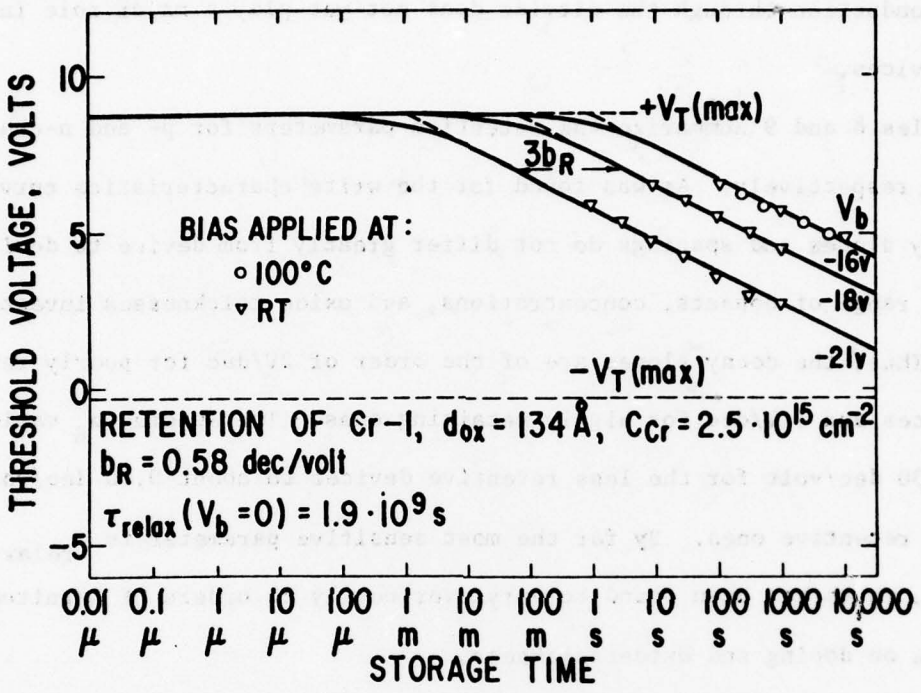


Figure 31. Retention of Chromium Doped P-Channel Memory Device

It should be noted that several of the measurements in Fig. 31 were carried out at 100°C instead of room temperature. These points coincide with the room temperature measurements indicating that at 100°C activated charge conduction through the nitride does not yet play a major role in these devices.

Tables 8 and 9 summarize the retention parameters for p- and n-channel devices, respectively. As was found for the write characteristics curves, the decay slopes and spacings do not differ greatly from device to device over the range of dopants, concentrations, and oxide thicknesses investigated. Thus, the decay slopes are of the order of 2V/dec for poorly retaining devices and 1 V/dec for highly retaining ones. The spacing b_R varies from about 0.30 dec/volt for the less retentive devices to about 0.60 dec/volt for the more retentive ones. By far the most sensitive parameter is τ_{relax} ($V_b = 0$), which has been found to vary over nearly 20 orders of magnitude depending on doping and oxide thickness.

The retention behavior of n-channel interface doped devices is quite analogous to that of p-channel devices. Figures 32 and 33 show the accelerated decay of the more positive threshold state for iridium and platinum doped n-channel varactors, respectively. It is seen that the retention can also be characterized by a set of parallel decay curves displaced from each other by the spacing b_R, and the intercepts τ_{relax} ($V_b = 0$) and t_R. In fact, the values of the retention parameters are very similar for p- and n-channel devices.

THE EFFECT OF OXIDE THICKNESS

τ_{relax} ($V_b = 0$) for the chromium doped device described in Fig. 31 is 1.9×10^9 seconds, or 60 years. This is not an uncommonly high value. Table

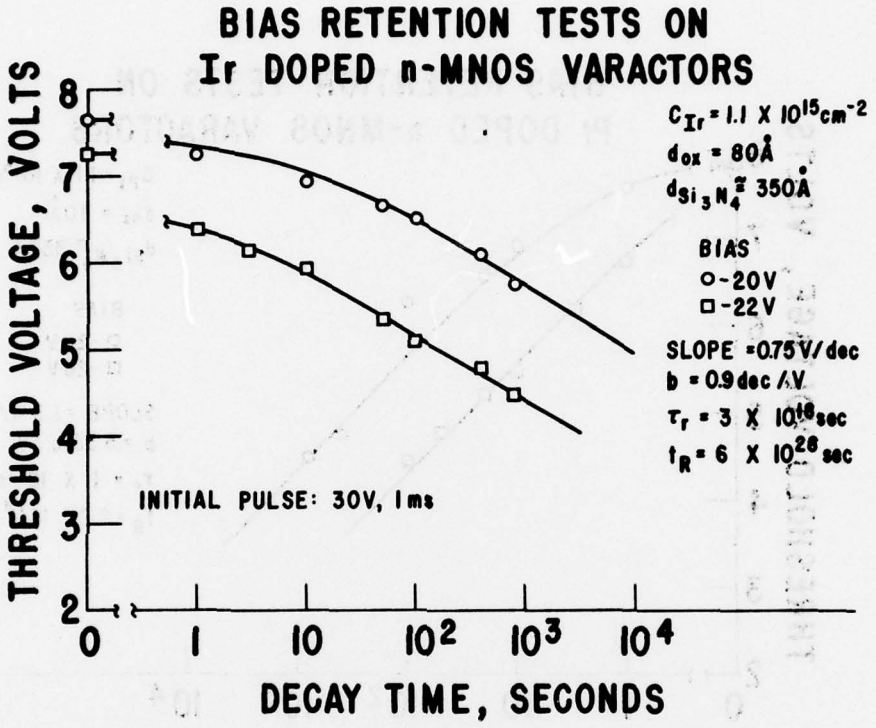


Figure 32. Retention of Iridium Doped N-Channel Memory Device

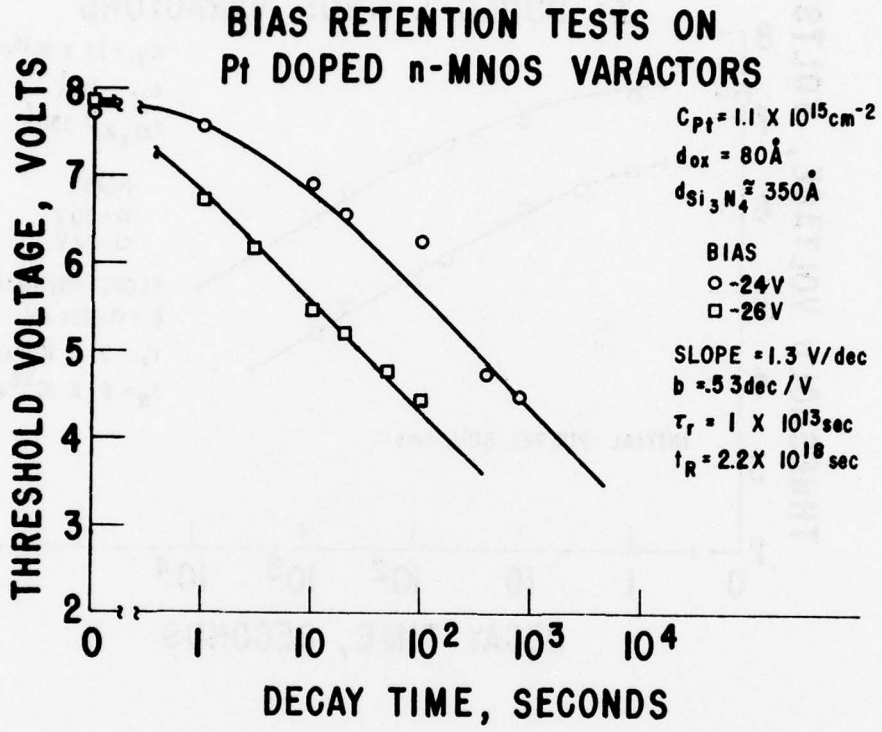


Figure 33. Retention of Platinum Doped N-Channel Memory Device

TABLE 8

RETENTION PARAMETERS FOR THE SIX DOPANTS, P-CHANNEL DEVICES

Dopant	Dop. conc. $\times 10^{15}$ cm^{-2}	d_{ox}, Å	b_R, dec/volt	Decay slope volt/dec	Retention τ_{relax}, secs	V_T initial*	t_R, sec
Cr-1	8.6	53	0.18	2.1	3×10^{1}	10V	3.2×10^{5}
"	2.95	53	0.36	2.7	3.5×10^{4}	10V	4.2×10^{7}
"	8.6	134	0.48	1.1	3.0×10^{5}	10V	5.7×10^{14}
"	2.95	134	0.58	1.1	5.0×10^{8}	10V	4.7×10^{17}
Cr-2	0.77	61	0.62	1.2	1.0×10^{10}	7V	1.2×10^{15}
"	0.77	134	0.50	1.2	5.0×10^{9}	7V	3.2×10^{14}
Cr-14 in	5.2	36	-	1.18	8×10^{1}	~ 4V	4.0×10^{5}
-14 in	1.1	36	-	1.18	5.3	3.5V	5.0×10^{3}
-15 in	1.1	50	0.45	1.13	8.7×10^{5}	5.3V	4.0×10^{10}
-15 in	5.4	50	0.45	1.4	1.0×10^{7}	5.2V	4.6×10^{10}
-14 out	5.2	43	-	1.0	8.5×10^{1}	5.4V	1.1×10^{8}
-14 out	1.1	43	0.38	1.34	3.1×10^{3}	5.15V	1.2×10^{7}
-15 out	1.1	57	1.0	0.68	8.0×10^{10}	5.2V	4.0×10^{18}
-15 out	5.4	57	1.0	0.72	3.0×10^{9}	5.7V	4.1×10^{17}
W-17	1.4	59	0.15	3.8	8.3×10^{2}	6.5V	4.0×10^{4}
"	0.23	59	0.13	3.8	3.2×10^{3}	6.5V	1.7×10^{5}
W-39	0.55	63	0.60	1.0	3.1×10^{12}	6.0V	1.0×10^{18}
"	2.5	63	0.34	1.8	7.6×10^{6}	6.0V	6.3×10^{9}
"	0.77	103	0.703	1.3	2.7×10^{17}	6.0V	4.5×10^{21}
"	2.5	103	0.46	2.1	6.3×10^{9}	6.0V	6.3×10^{12}
W-40	0.22	85	0.725	1.1	2.0×10^{11}	3.7V	8.8×10^{19}
-44 in	1.08	68	0.59	1.34	1.0×10^{9}	8.0V	3.0×10^{13}
-45 in	2.8	68	0.775	1.1	6.0×10^{14}	8.2V	1.1×10^{20}
-47	1.8	84	0.47	0.9	1.7×10^{7}	5.05V	2.2×10^{12}
-48	1.94	72	0.83	1.0	6.0×10^{11}	6.4V	2.9×10^{13}
"	1.94	58	0.64	1.27	4.8×10^{8}	6.35V	7.8×10^{13}
Ir-2	0.081	53	0.30	1.9	2.5×10^{4}	8V	4.0×10^{8}
"	0.081	80	0.67	1.1	2.3×10^{12}	8V	1.0×10^{19}
Ir-1	1.09	80	0.39	1.6	1.8×10^{6}	8V	6.0×10^{11}
"	1.09	53	-	1.7	5×10^{-2}	8V	2.0×10^{3}
Ir-7	0.15	72	0.73	0.88	6.8×10^{9}	4.85V	6.3×10^{12}
"	0.15	58	0.63	0.65	1.4×10^{6}	4.05V	1.2×10^{14}
Ni-4	0.266	53	0.31	1.3	1.7×10^{5}	8V	1.7×10^{11}
"	1.22	53	0.35	1.6	2.1×10^{4}	8V	2.1×10^{9}
"	0.266	85	0.77	0.7	1.3×10^{10}	8V	1.0×10^{19}
"	1.22	85	0.91	0.8	1.2×10^{12}	8V	1.0×10^{21}
Ni-10	2.37	72	0.75	0.94	9.0×10^{7}	4.7V	7.3×10^{12}
"	0.53	58	0.88	0.63	5.8×10^{8}	4.05V	1.2×10^{15}
Pd-1	1.85	70	0.16	2.1	1.0×10^{2}	7.5V	1.0×10^{6}
"	3.5	70	0.41	1.6	5.0×10^{3}	7.5V	1.0×10^{8}
"	1.85	100	0.26	1.3	1.6×10^{4}	4V	1.6×10^{8}
"	3.5	100	0.33	0.73	6.0×10^{5}	4V	6.0×10^{9}
Pt-10	0.37	61	0.33	1.71	3.0×10^{3}	7V	3.0×10^{7}
"	0.37	88	0.86	0.80	2.4×10^{12}	7V	2.0×10^{20}
"	1.94	70	0.69	0.90	6.5×10^{11}	7V	1.0×10^{18}
"	1.94	100	0.57	1.11	3.5×10^{9}	7V	3.5×10^{15}

TABLE 8, Concluded

Dopant	Dop. conc. x 10^{15} cm^{-2}	d_{ox}, Å	b_R, dec/volt	Decay slope volt/dec	Retention		
					τ_{relax}, secs	V_T initial*	t_R, sec
Pt-11	1.1	85	1.0	0.67	2.2×10^{14}	5.2V	1.3×10^{21}
"	0.27	85	0.95	1.7	1.7×10^{13}	4.8V	6.0×10^{19}
Pt-16	0.16	72	1.18	0.52	1.2×10^{11}	4.4V	2.6×10^{14}
"	0.12	58	0.7	0.65	3.0×10^{6}	3.8V	2.4×10^{12}
Pd-3	0.18	85	1.13	0.42	2.6×10^{12}	3.8V	8.0×10^{20}
"	1.58	85	1.1	0.4	4.0×10^{13}	3.5V	1.1×10^{22}
Cr-4	0.81	85	0.87	0.77	5.1×10^{11}	5.1V	2.0×10^{18}
"	3.9	85	0.76	1.0	3.5×10^{10}	5.5V	9.0×10^{15}

* Positive threshold voltage from which decay is measured.

TABLE 9

RETENTION PARAMATERS FOR THREE DOPANTS, N-CHANNEL DEVICES

Dopant	Dopant Conc. $\times 10^{15}$ cm^{-2}	d_{ox}, Å	b_R, dec/V	Decay slope V/dec	Retention τ_{relax}, secs	Retention V_T initial, V	Retention t_R, sec
Pt	0.7	64	.5	1.5	6×10^{11}	9.1	8×10^{17}
	0.3	"	.53	1.2	3×10^{9}	9.5	4×10^{17}
	1.1	"	.66	0.9	2.5×10^{13}	8.5	6×10^{22}
	0.7	80	.45	1.4	2.1×10^{10}	8	6×10^{16}
	1.1	"	.53	1.3	1×10^{13}	7.8	2.2×10^{18}
	0.3	"	.48	1.2	1.7×10^{9}	8.6	2×10^{16}
	2.7	85	.5	1.3	8×10^{4}	5.8	2.1×10^{9}*
	0.2	"	0.72	0.65	8.5×10^{7}	5.7	1×10^{17}
Ir	0.7	80	.65	0.7	1×10^{13}	8	1×10^{24}
	0.3	"	.61	0.75	2×10^{10}	9	8×10^{20}
	1.1	"	.9	0.75	3×10^{18}	7.6	6×10^{28}
	0.7	64	.61	0.8	2.5×10^{12}	8.8	6×10^{22}
	0.3	"	.4	1.2	8×10^{6}	10.3	4×10^{15}
	1.1	"	.5	0.6	3×10^{8}	8.5	8×10^{22}
Cr	1.3	85	.38	2.4	1.1×10^{4}	9.9	3.5×10^{2}
	0.6	"	1.2	.67	1×10^{14}	5.4	1.1×10^{22}
	0.6	64	.59	.8	5×10^{12}	6.6	9×10^{20}
	2.5	"	.75	.65	4×10^{18}	5.4	6×10^{26}
	1.5	"	.54	.7	6×10^{12}	5.9	4×10^{20}
	2.5	80	.86	.95	2×10^{23}	5.6	1×10^{29}
	1.5	"	.49	.9	7×10^{12}	5.6	8×10^{18}
	0.6	"	.6	1.35	5×10^{13}	7.0	1×10^{19}

* 1 ohm-cm wafers

8 contains a list of the four important retention parameters, including τ_{relax} ($V_b = 0$), for devices studied in the course of Phase I of this program. τ_{relax} ranges from a low of 5.3 seconds to 8.5×10^9 years. This extreme variation in charge retention is largely a function of oxide thickness. If devices are compared in Table 8 which have the same dopant and concentration, there are many examples where the device with the thicker oxide has the higher retention.

Figure 34 illustrates the relationship between oxide thickness and τ_{relax} and t_R for chromium doped devices. It can be seen that they depend strongly on oxide thickness.

THE EFFECT OF DOPANT CONCENTRATION

The decay of a written threshold voltage at some applied gate bias is at first quite rapid (linear portion on the log time plot), but then, as it approaches zero volts, the decay becomes much slower (nonlinear in log time). It is the rapid, linear decay which was described above, and which is used to estimate τ_{relax} and t_R. The slope of this curve (V/dec) increases slightly as the dopant concentration increases. In addition, there is a slight increase in the decay slope with the applied bias voltage. This is shown in Table 10 in which the decay slope is shown as a function of Cr dopant concentration and bias voltage, for constant oxide and nitride thicknesses of 70 Å and 452 Å, respectively. The increase in the decay slope is more rapid with concentration for thicker oxide layers.

It can be seen from Table 8 that b_R generally depends strongly on the oxide thickness, increasing with thickness, for p-channel devices. There is also a dependence on the concentration at any one oxide thickness. This is even more clearly brought out in Table 11, where b_R is listed as a function of Cr dopant concentration for 100 Å oxide and 452 Å nitride devices. It is

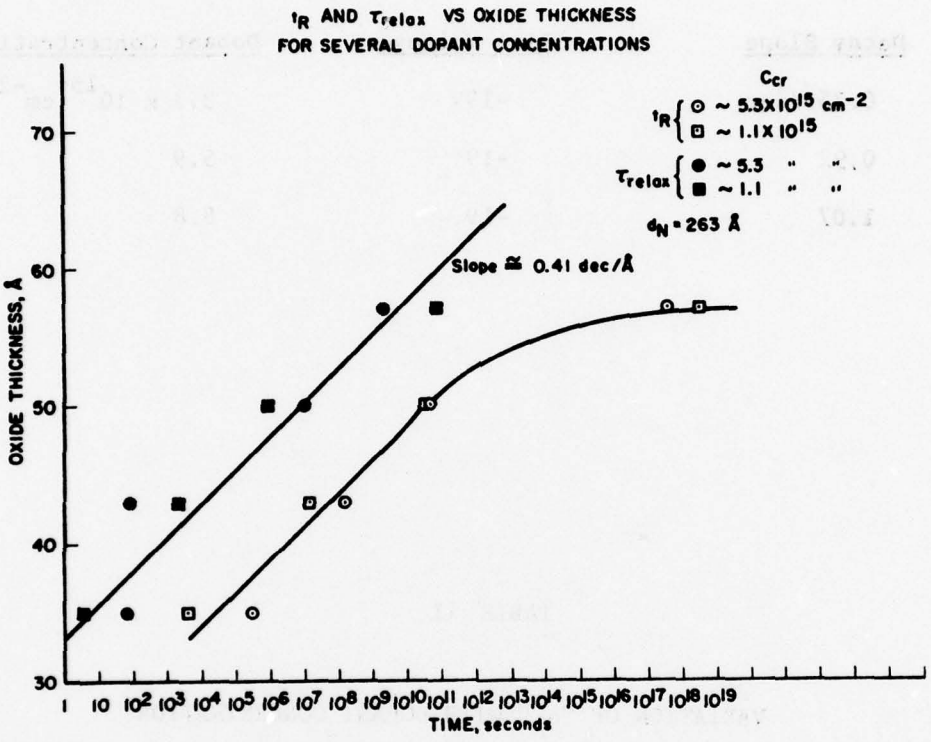


Figure 34. t_R and τ_{relax} vs. Oxide Thickness

TABLE 10

VARIATION OF DECAY SLOPE WITH CONCENTRATION

OF DOPANT AT 70A OXIDE THICKNESS (P-CHANNEL)

Decay Slope	Bias Voltage	Dopant Concentration
0.75V/dec	-19V	3.3×10^{15} cm^{-2}
0.92	-19	5.9
1.07	-19	8.8

TABLE 11

VARIATION OF "b_R" WITH DOPANT CONCENTRATION

AT 100A OXIDE THICKNESS (P-CHANNEL)

Dopant Concentration	-19V & -21V	-19V & -25V	-21V & -25V
1.8×10^{15} cm^{-2}	0.75 dec/V	0.64 dec/V	0.59 dec/V
5.9	0.53	0.54	0.55
8.8	0.22	0.11	0.27

AD-A068 493 GENERAL ELECTRIC CORPORATE RESEARCH AND DEVELOPMENT --ETC F/G 9/1
INTERFACE DOPING OF MNOS TRANSISTORS.(U)
JUN 78 C A NEUGEBAUER, M M BARNICLE F33615-76-C-1035

UNCLASSIFIED SRD-78-097 AFAL-TR-78-87 NL

2 OF 3
AD
A068493

seen that between 1.8 and $5.9 \cdot 10^{15}$ cm^{-2}, b_R decreases only slowly, but it decreases rapidly as the concentration increases above $5.9 \cdot 10^{15}$ cm^{-2}. It is also seen in Table 11 that b_R is a slow function of the bias voltage applied during the accelerated retention measurement, increasing with decreasing bias. This means that the estimates made in Table 8 to obtain τ_{relax} (V_b = 0) and t_R are conservative.

The effect of dopant concentration on the decay slope and b_R of p-channel devices is illustrated in Fig. 35. As the dopant concentration increases, τ_{relax} decreases for several oxide thicknesses and applied voltages, as a result of a decreasing b_R and increasing decay slope.

For n-channel memory devices, the dependence of the dopant concentration on τ_{relax} changed slopes. This can be seen by comparing Fig. 34 with Fig. 36, which shows the effect of dopant concentration on τ_{relax} for n-channel devices. It is seen that while τ_{relax} increases with increasing chromium concentration for p-channel devices, it decreases within increasing chromium concentration for n-channel devices.

TEMPERATURE DEPENDENCE

As pointed out above, one possible charge decay mechanism, namely conduction through the nitride, is strongly temperature dependent. However, it was found here that within the temperature range studied, -196°C to 250°C, back tunneling is the dominant mechanism.

Figure 37 contains several retention plots, each carried out at a different temperature. The same applied bias was used in each case and all devices were originally written at room temperature. It can be seen that decay at each temperature occurs at virtually the same rate. The decay slope is independent of temperature between room temperature and 200°C. Since τ_{relax} is a function not only of the decay slope but also of b_R, another

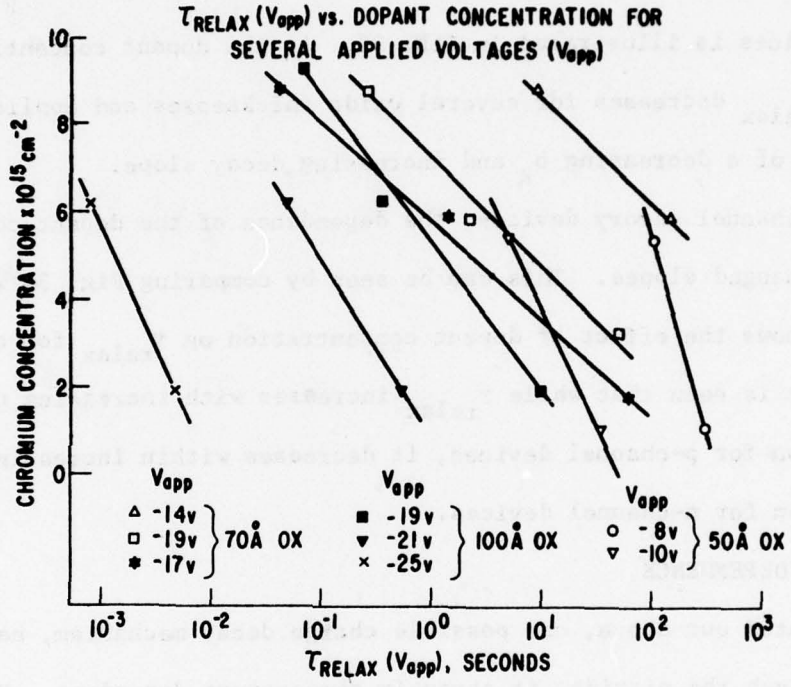


Figure 35. τ_{relax} (V_{app}) vs. Dopant Concentration, P-Channel Devices

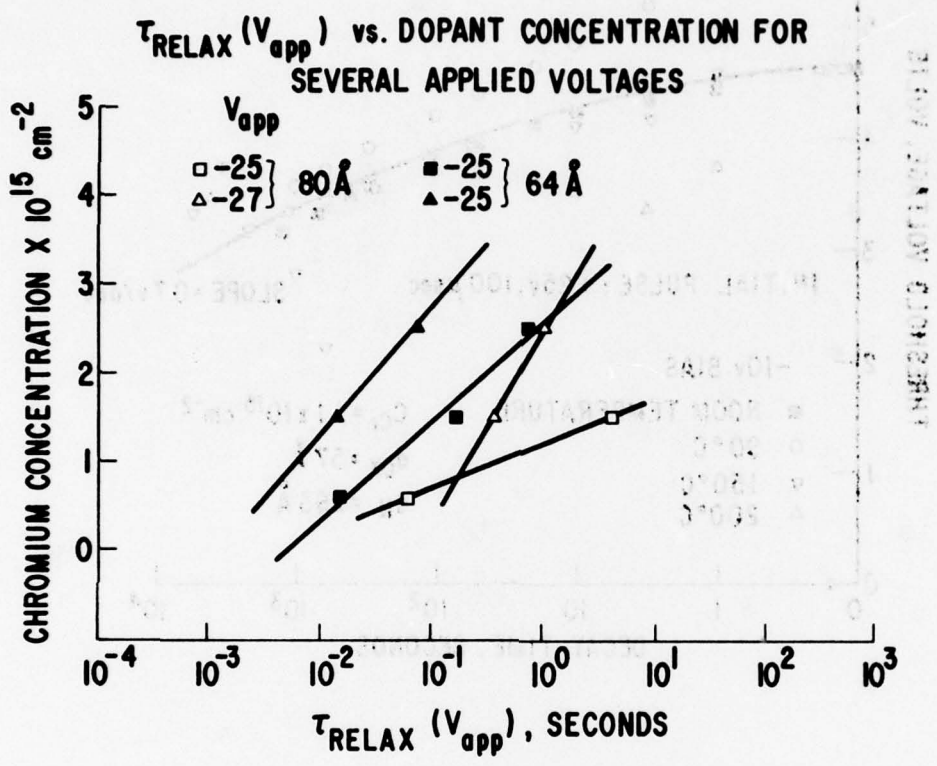


Figure 36. τ_{relax} (V_{app}) vs. Dopant Concentration, N-Channel Devices

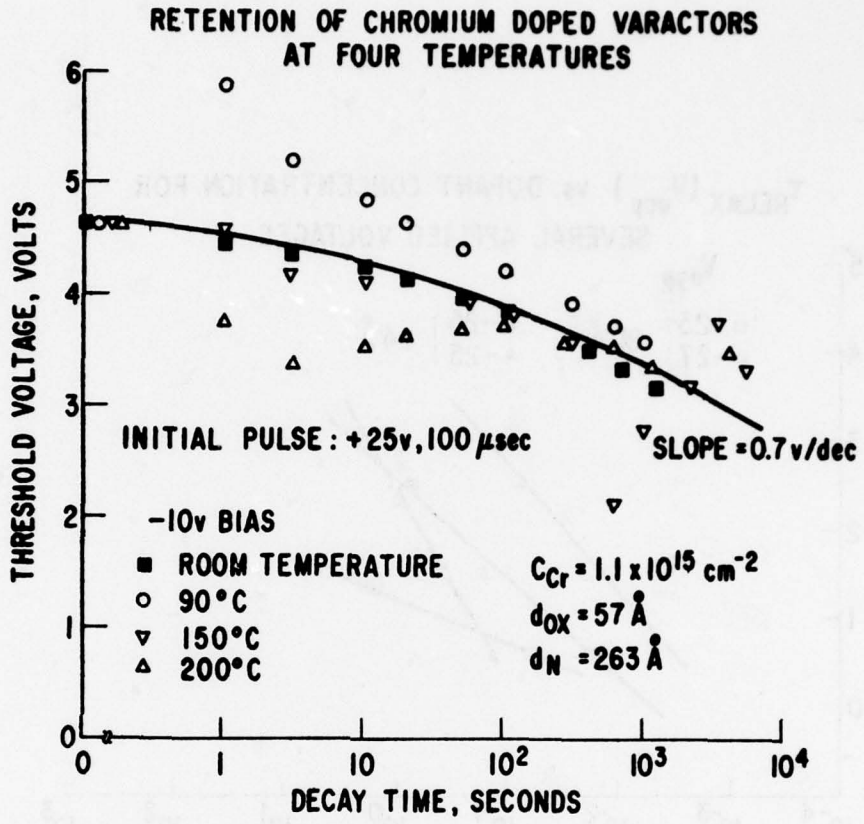


Figure 37. Chromium Retention at Four Temperatures for P-Channel Devices

experiment was carried out to determine how the separation between decay curves at different biases is affected by temperature. The results are shown in Fig. 38. Retention measurements were made with three different bias voltages at both room temperature and 250°C. As can be seen, threshold voltage values for a particular bias cluster together for both temperatures. It is thus concluded that b_R is also not strongly affected by temperature, at least to a first order approximation.

To further test the temperature dependence, retention tests were made at liquid nitrogen temperature. Figure 39 contains the results of two retention tests. In one test the bias voltage was applied at room temperature. In the second test, bias was applied at 77°K. This curve was corrected for a voltage shift due to fast surface state generation (see below). Even at 77°K therefore, charge decay does not occur at a significantly different rate than at room temperature, indicating charge decay due to back tunneling only.

The retention of n-channel memory devices at higher temperatures parallels that of p-channel devices. This is illustrated in Figs. 40, 41 and 42. Figure 40 shows that,when written at the same temperature, the decay of the memory is not strongly temperature dependent, indicating that back tunneling is the important mechanism in stored charge decay for n-channel as well as p-channel devices.

Writing at a higher temperature is normally followed by a positive threshold surge at bias times less than one second, as seen in Figs. 40 and 41, but the decay behavior is similar at all temperatures. Even when the devices are written at higher temperature, the threshold voltage decay with time has the same bias voltage dependence as described above for room temperature. This is illustrated in Fig. 42.

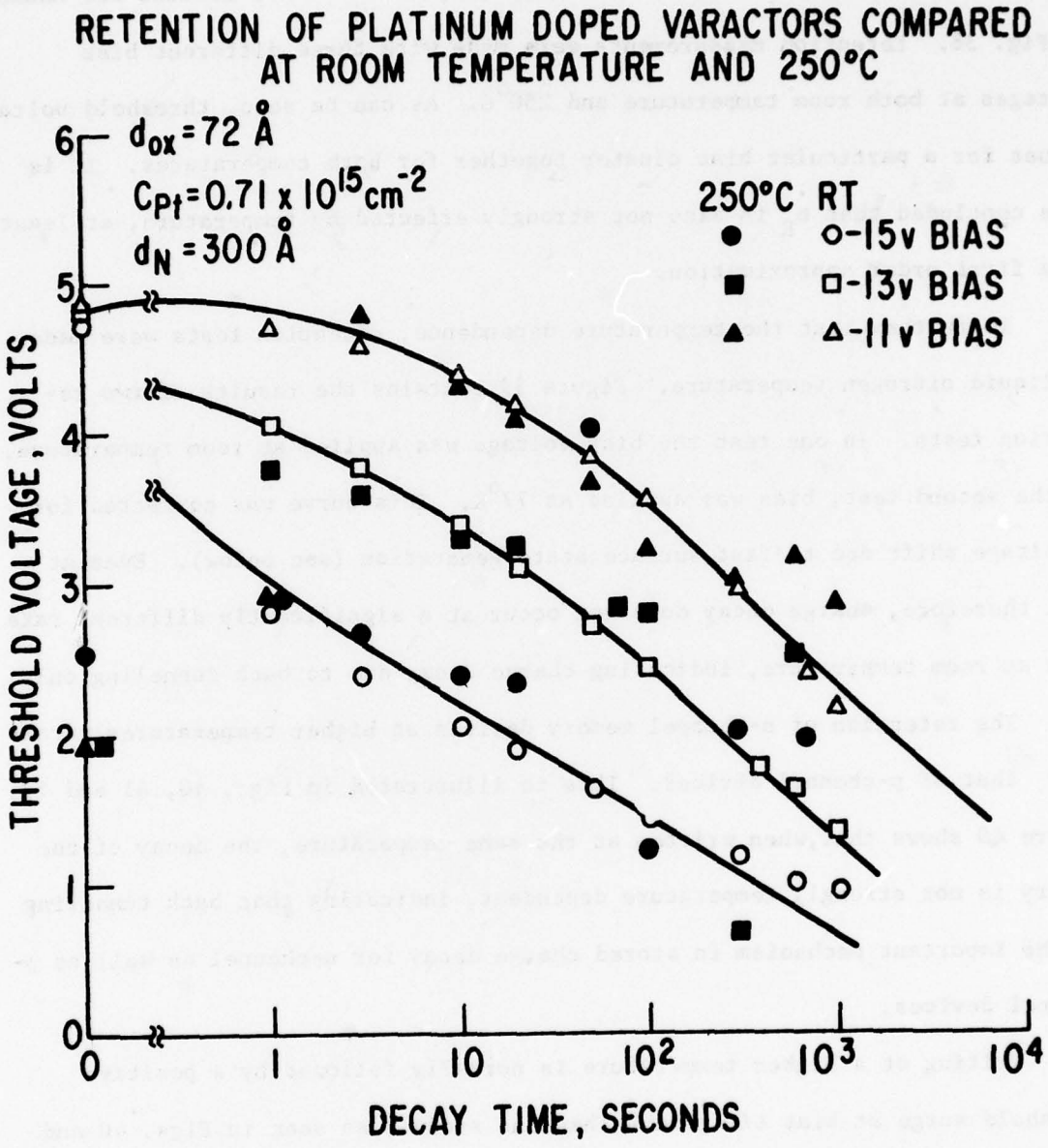


Figure 38. Platinum Retention at Room Temperature and 250°C for P-Channel Devices

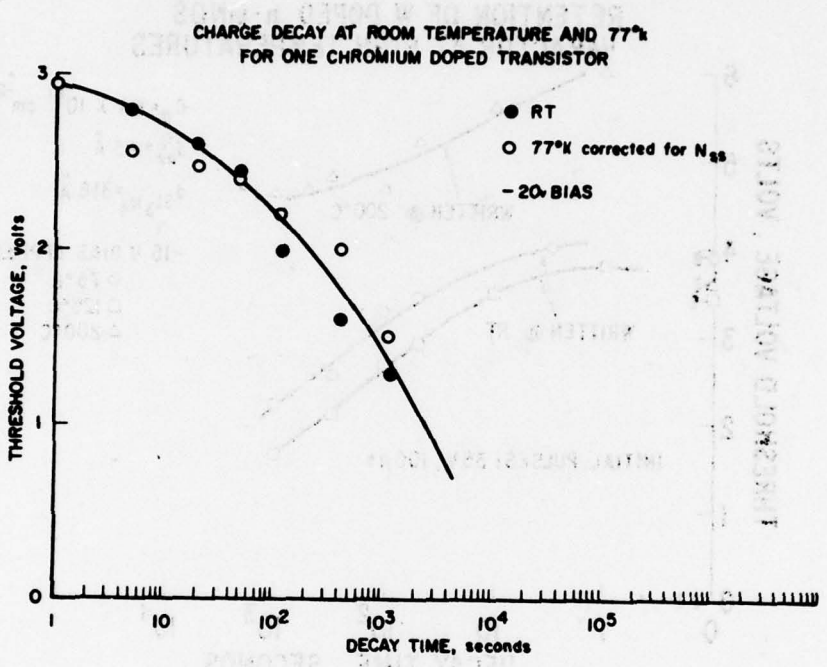


Figure 39. Charge Decay at Room Temperature and 77°K

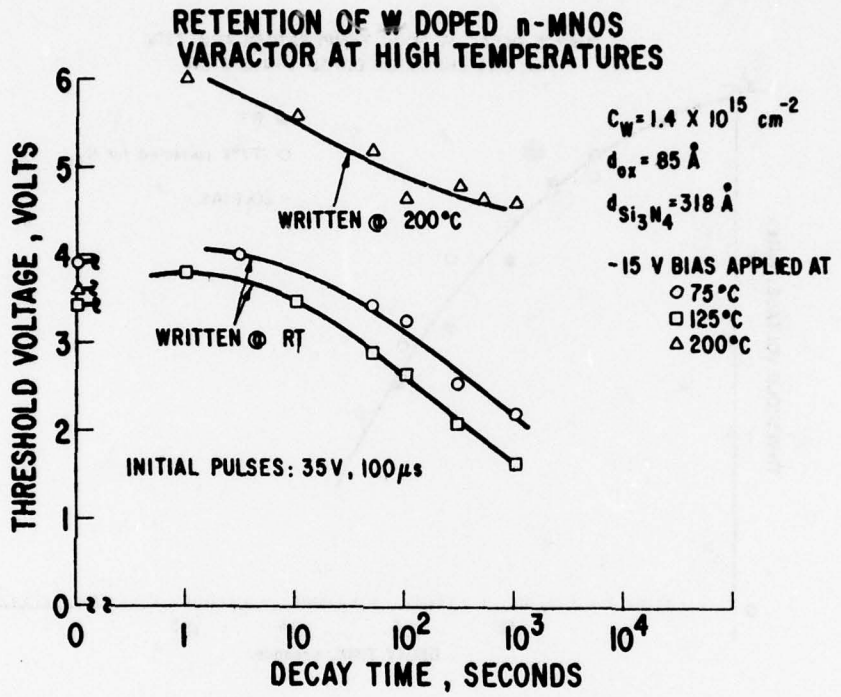


Figure 40. Tungsten Retention at Three Temperatures for N-Channel Devices

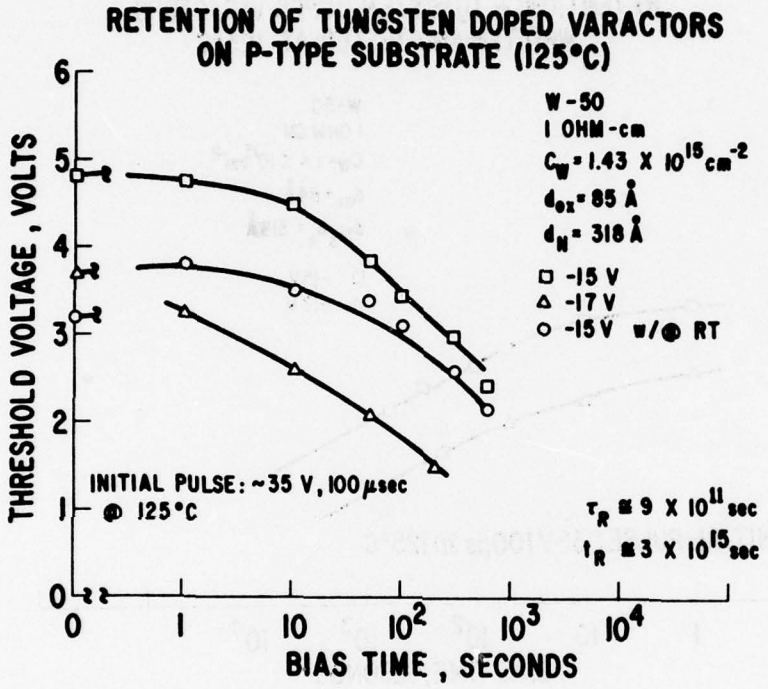


Figure 41. Tungsten Retention at 125°C for N-Channel Devices

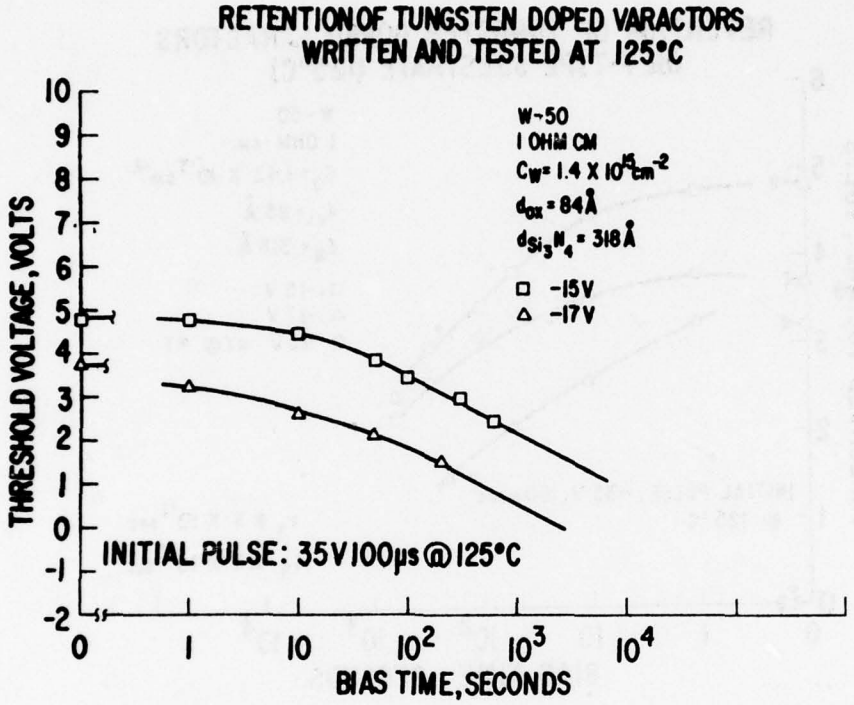


Figure 42. Tungsten Retention at 125°C for N-Channel Devices

In conclusion, the retention of metal doped MNOS devices is independent of temperature between -196°C and 250°C, at least to a first order approximation. Writing at higher temperatures does not change the retention characteristics.

THE EFFECT OF HIGH POSITIVE APPLIED VOLTAGES

Most retention tests are made at room temperature and with applied biases that are considered low when compared to the voltages used to write the devices. To obtain a maximum decay rate, negative biases were used mostly for retention tests. However, the effect of positive bias on charge decay was also investigated for several dopants. The results for palladium doped varactors are shown in Fig. 43. Back tunneling of the electrons through the oxide (negative bias) is still clearly the faster decay mechanism. However, at +20 volts bias, the threshold also decays in a negative direction at room temperature. This cannot be due to back tunneling, since positive bias should yield a positive threshold shift. A positive shift would be expected if conduction through the nitride is taking place. However, that mechanism is highly activated, and has not been observed (Figs. 37 and 38). The positive shift is thus believed to be caused by the third threshold shift mechanism, which is always characterized by the formation of large numbers of fast surface states. As demonstrated in Fig. 43, measurements at room temperature and 77°K show the generation of such surface states with time, as shown by the divergence of the 77°K and R.T. decay curves at longer times. (See Section VIII.) Indeed, after 100 seconds of applied bias, surface states are increasing at a rapid rate.

Platinum doped varactors showed similar results. In Fig. 44, note again that back tunneling is the fastest decay mechanism. At positive bias, more and more surface states are generated with time. No surface state formation occurs for comparable negative biases.

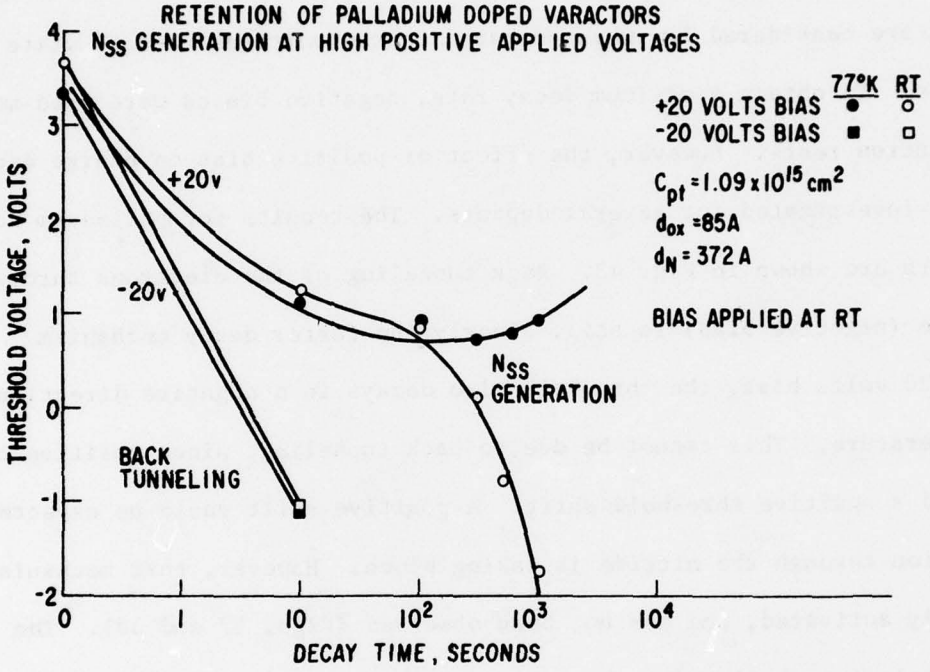


Figure 43. Palladium Retention at High Positive Applied Voltages, P-Channel Devices

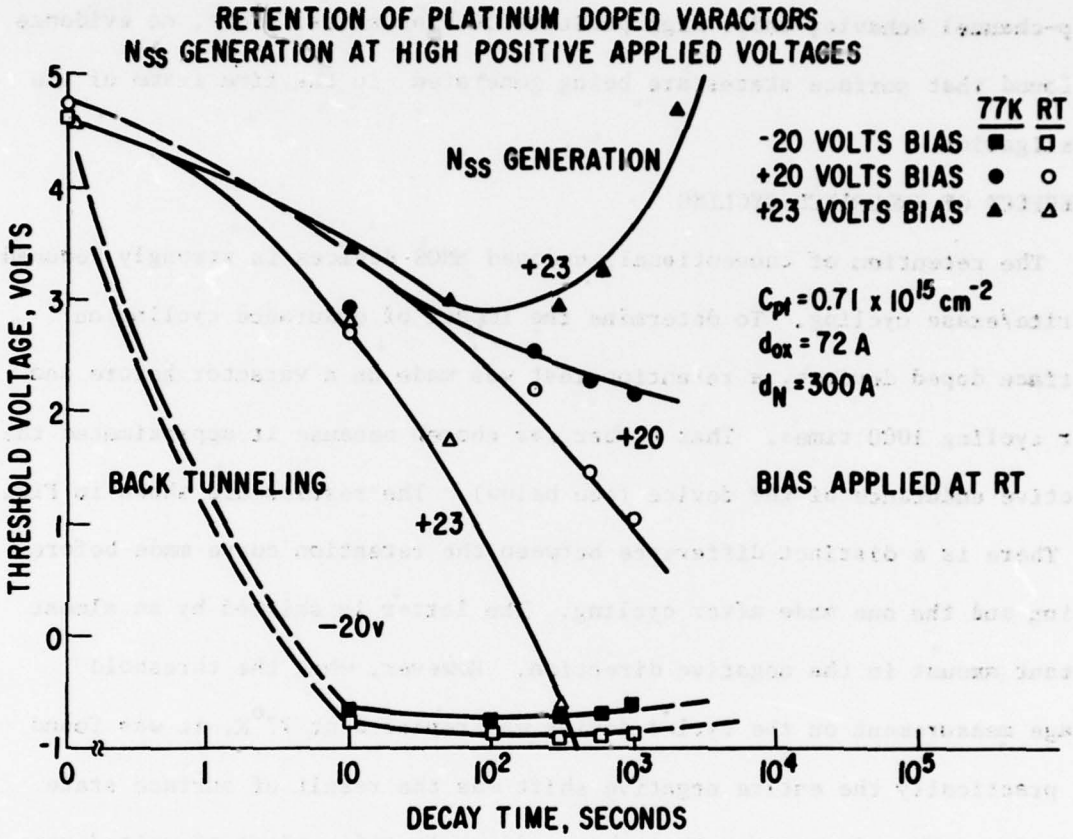


Figure 44. Platinum Retention at High Positive Applied Voltages, P-Channel Devices

For n-channel devices, a high positive DC bias also leads to a lowering of the threshold voltage. This is illustrated for a tungsten doped varactor in Fig. 45 and a platinum doped varactor in Fig. 46. However, in contrast to the p-channel behavior under high positive DC bias stress above, no evidence was found that surface states are being generated in the time frame of the investigation.

THE EFFECT OF ENDURANCE CYCLING

The retention of conventional, undoped MNOS devices is strongly reduced by write/erase cycling. To determine the impact of endurance cycling on interface doped devices, a retention test was made on a varactor before and after cycling 1000 times. That number was chosen because it approximated the effective endurance of the device (see below). The results are shown in Fig. 47. There is a distinct difference between the retention curve made before cycling and the one made after cycling. The latter is shifted by an almost constant amount in the negative direction. However, when the threshold voltage measurement on the cycled device was repeated at $77^{o}K$, it was found that practically the entire negative shift was the result of surface state generation. Thus it appears that charge decay is independent of write/erase cycling to 1000 cycles, but the formation of surface states during cycling causes the room temperature threshold voltage to be reduced. Fast surface state generation in relation to write/erase cycling is discussed in a later section.

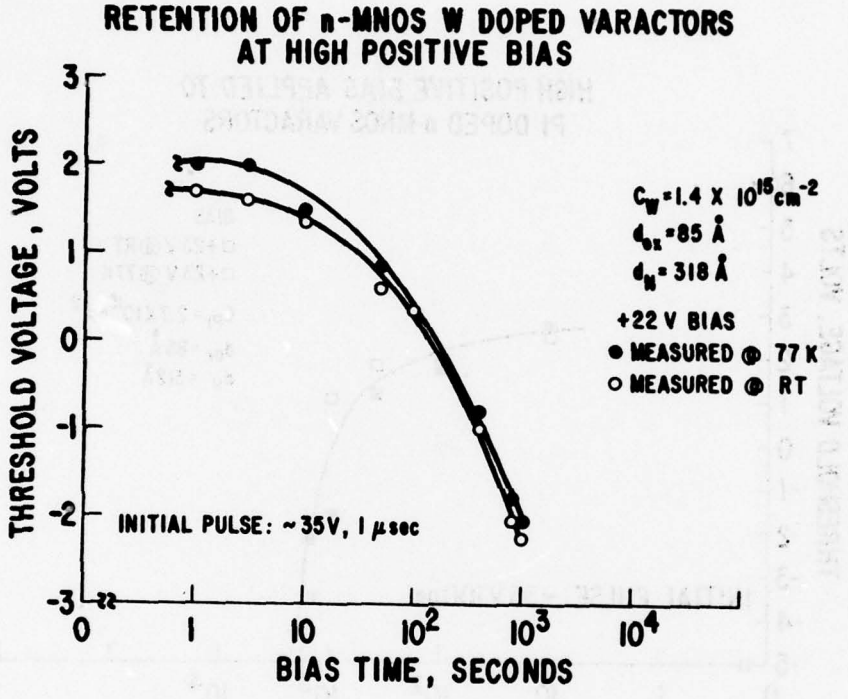


Figure 45. Tungsten Retention at High Positive Applied Bias

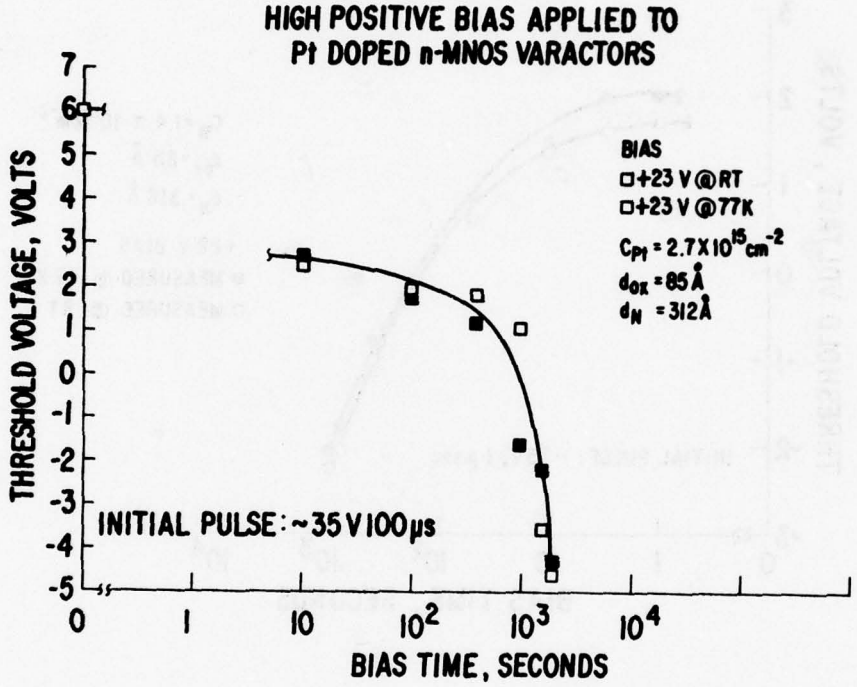


Figure 46. Platinum Retention at High Positive Applied Bias

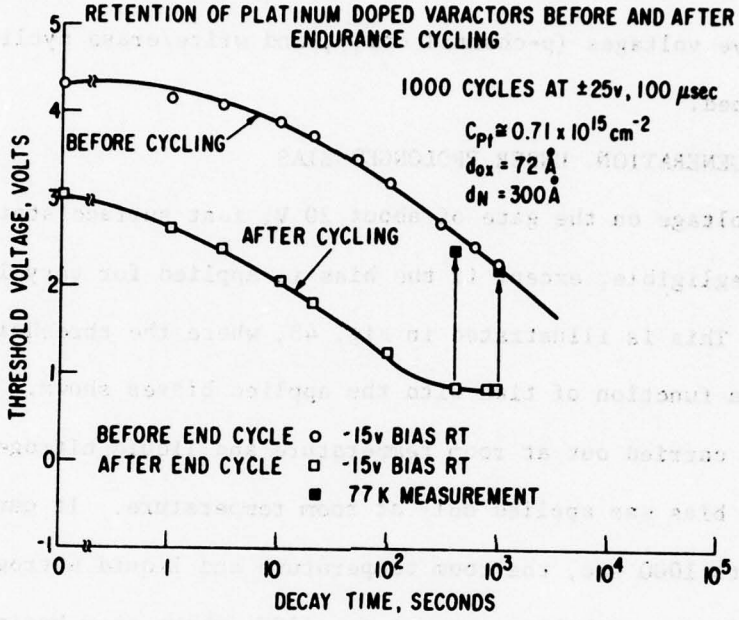


Figure 47. Platinum Retention Before and After Endurance Cycling (P-Channel)

SECTION VIII

FAST SURFACE STATE GENERATION

It was found in the course of this study that fast surface states could be generated in interface doped devices by two methods: Prolonged application of high positive voltages (p-channel only), and write/erase cycling. These are now described.

SURFACE STATE GENERATION UNDER PROLONGED BIAS

Up to a voltage on the gate of about 20 V, fast surface state generation is generally negligible, except if the bias is applied for very long times ($>$ 1000 sec). This is illustrated in Fig. 48, where the threshold voltage is plotted as a function of time with the applied biases shown. The measurement of V_T was carried out at room temperature and liquid nitrogen temperature, but the bias was applied only at room temperature. It can be seen that at least to 1000 sec, the room temperature and liquid nitrogen threshold roughly coincide for each bias, except for +19V, where they begin to diverge from 100 sec on, indicating an increasing rate of surface state generation at that bias. We use here the method of Brown and Gray[3], which relates the density of fast states to the flat band voltage shift between room and liquid nitrogen temperature.

Devices on the same wafer were subjected to even higher bias, as shown in Fig. 49. Here a definite divergence of the liquid nitrogen and room temperature threshold voltages can be observed after about 30 sec, for positive voltages above +20V, indicating the generation of a very large number of fast surface states, rising to about 10^{13} cm^{-2} at 1000 sec. Note that no surface states are generated at -20V.

---

[3] P.V. Gray and D. M. Brown, Applied Physics Letters, Vol. 7, 108 (1965).

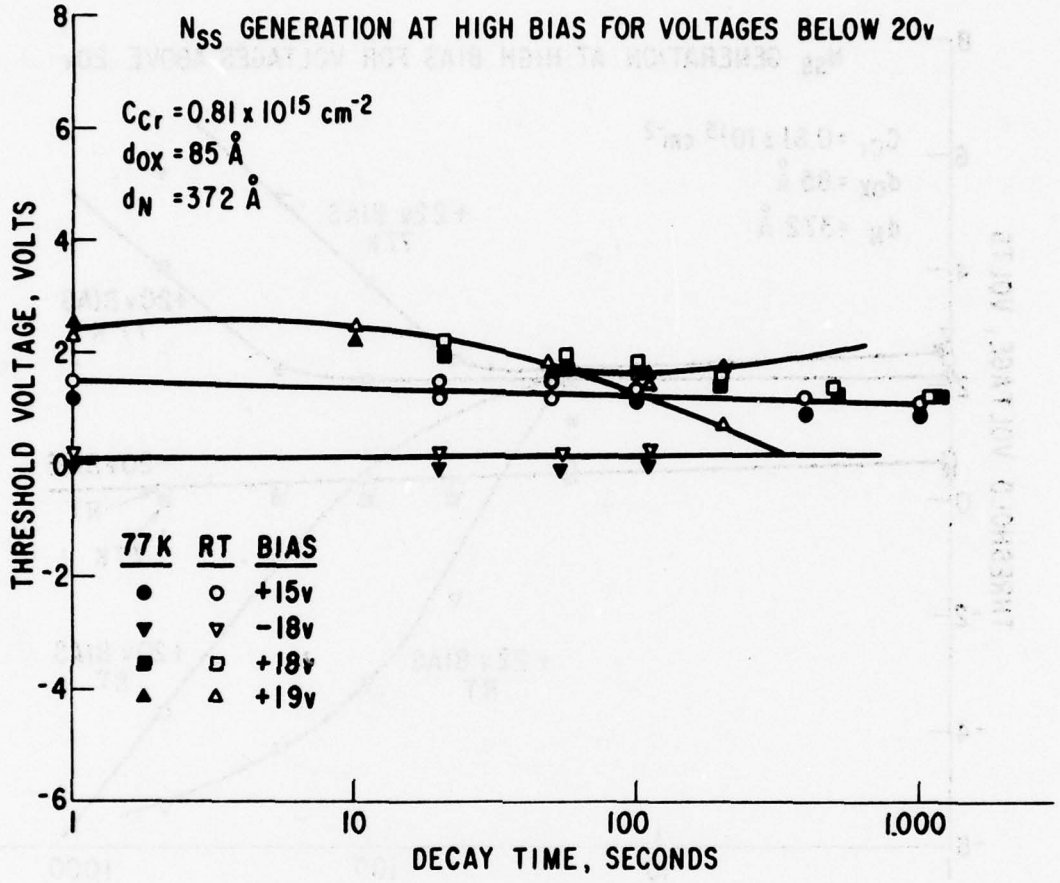


Figure 48. N_{ss} Generation at High Bias for Voltages Below 20V (P-Channel)

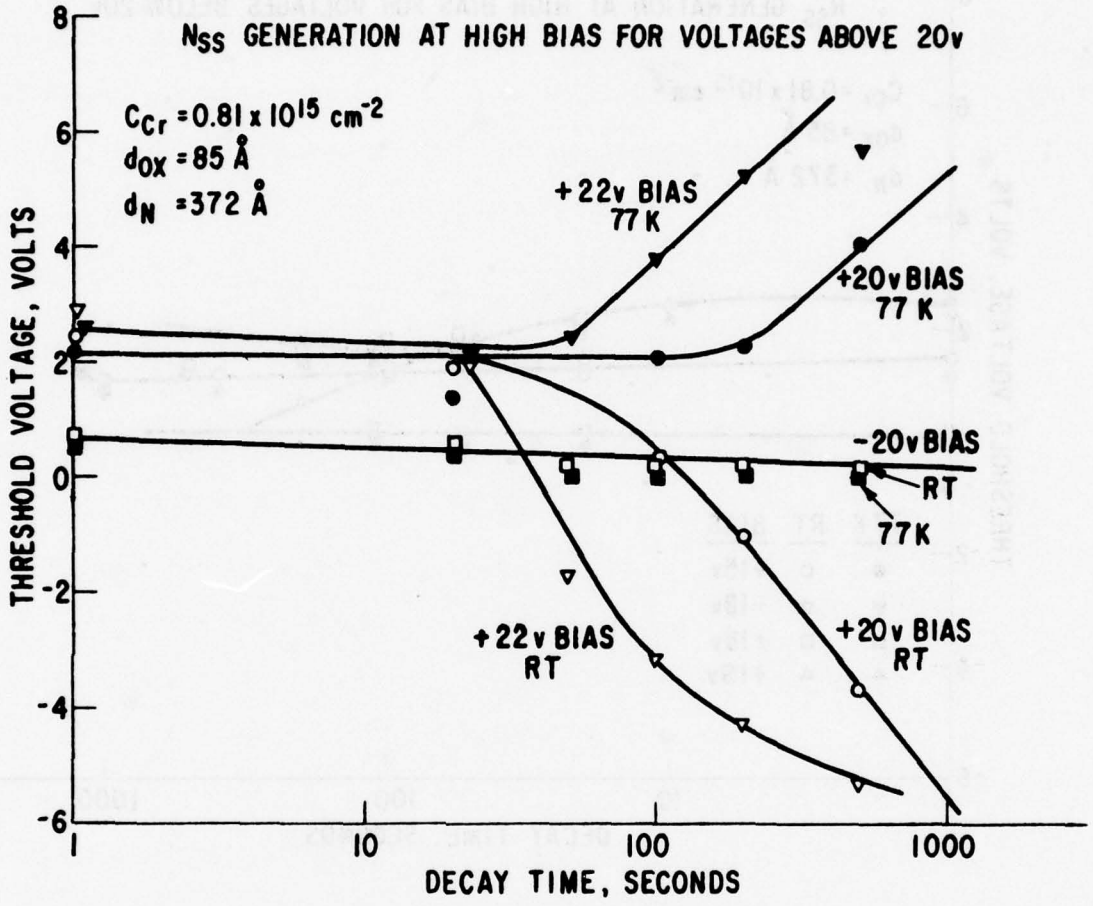


Figure 49. N_{ss} Generation at High Bias for Voltages Above 20V (P-Channel)

Figure 50 shows fast surface states generated at +25 in tungsten doped varactors.

SURFACE STATE GENERATION DUE TO WRITE/ERASE CYCLING

In write/erase cycling above 1000 cycles, severe distortion of the C-V curve is observed, indicating a large number of surface states. The surface state density of a chromium doped device is shown in Fig. 51 as a function of write/erase cycling. It can be seen that the surface state density increases sharply after 1000 cycles, increasing from $3 \cdot 10^{11}$ for the original device before cycling to $11.2 \cdot 10^{12}$ after 5000 cycles, and it increases at the same rate for both memory states.

In Fig. 52, the two memory states are plotted after they were measured at room temperature and liquid nitrogen temperature, as a function of the write/erase dose. It is observed that while the center voltage as measured at room temperature decreases with write/erase cycling, the center voltage as measured at liquid nitrogen temperature increases. However, the memory window is identical for the two temperatures up to at least 100 cycles. The number of write/erase cycles required for significant deviation of the center voltage and significant window closure coincides with the number of cycles at which the surface state density begins to increase sharply.

In Fig. 52, it can be seen that the behavior of the $-V_T$ memory state is quite different from that of the $+V_T$ state. At room temperature the $-V_T$ state remains about constant at -1V as write/erase cycling proceeds to 10^4 cycles. However, the same state remeasured at $77^{\circ}K$, shows increasingly more positive values beyond 100 cycles. The corresponding band diagram showing the introduction of surface states in the band gap is shown to the left in Fig. 53 .

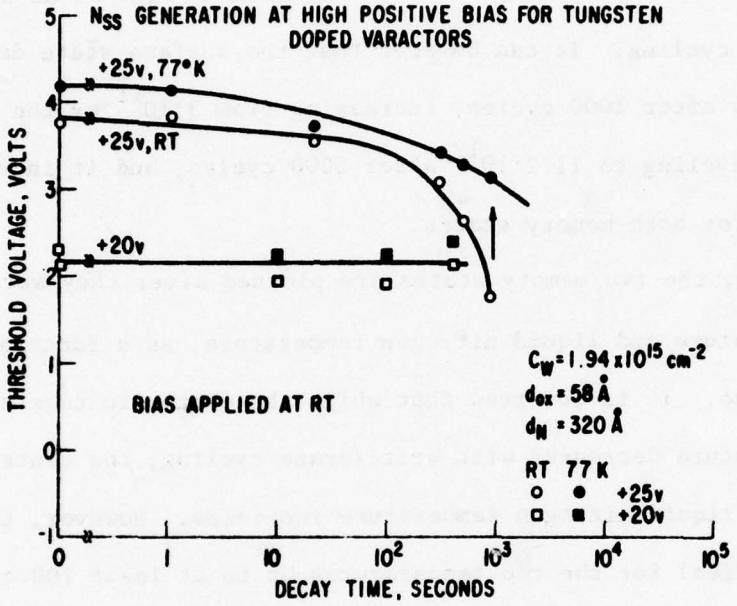


Figure 50. N_{ss} Generation at High Positive Bias for Tungsten Doped Varactors (P-Channel)

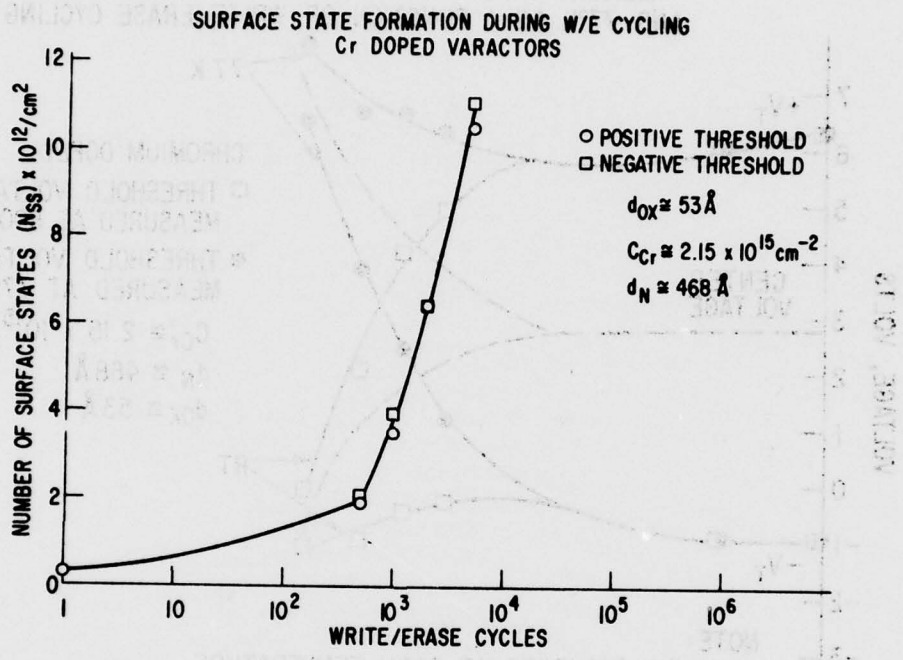


Figure 51. Surface State Formation During Write Erase Cycling (P-Channel)

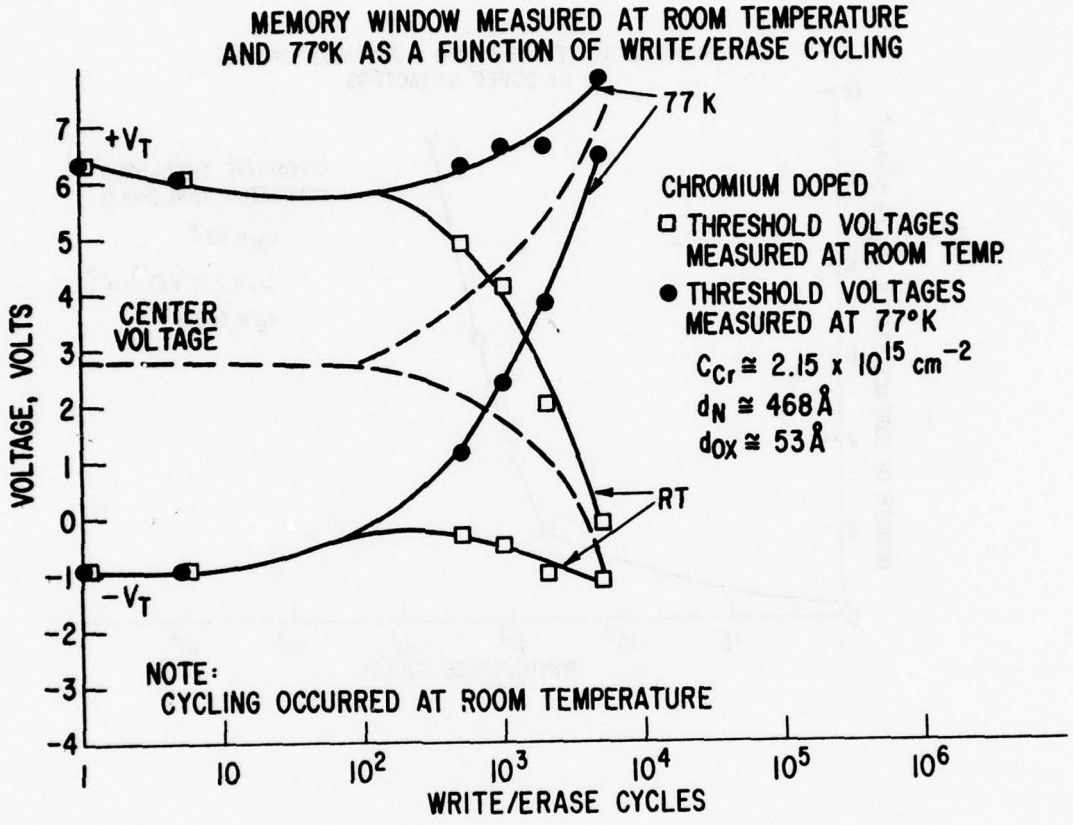


Figure 52. Memory Window Measured at Room Temperature and 77°K vs. Write/Erase Cycles (P-Channel)

The behavior is just reversed for the $+V_T$ memory state in Fig. 52. Here the room temperature value drops sharply with cycling beyond 100 cycles, while the 77°K value remains about constant at +7V. This situation requires a more complicated explanation than the $-V_T$ behavior. An attempt is made in the right half of Fig. 53. Here the surface states introduced in the band gap are accompanied by another set of positively charged states, which is perhaps similar in nature to "instability charge" postulated by others[4].

Surface state generation cannot be observed in n-channel devices, either under high positive DC bias or by write/erase cycling. Figure 54 shows the memory window of a chromium doped n-channel varactor measured at room temperature and 77°K as a function of write/erase cycling. In contrast to the p-channel equivalent in Fig. 52, no divergence of the data points for those two temperatures is observed, even for a high write/erase dose. The method of Brown and Gray[3] therefore leads to the conclusion that surface states are not generated in n-channel memory devices. Note, however, that this does not improve endurance greatly over p-channel devices. (See Section IX.)

[4] See, for instance, S. M. Sze, Physics of Semiconductor Devices, Wiley-Interscience, NY, 1969, p. 444.

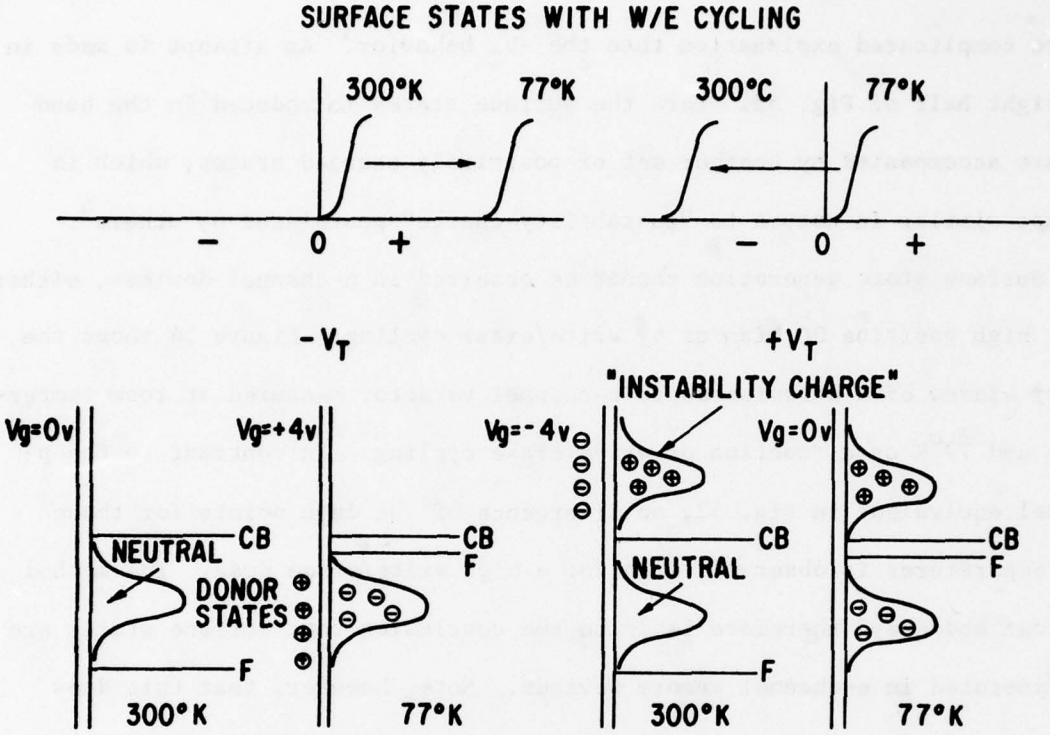


Figure 53. Surface States vs. Write/Erase Cycling for P-Channel Devices

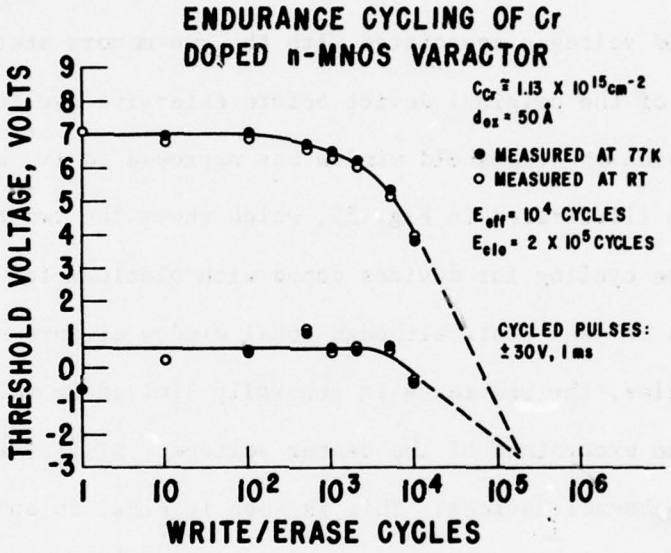


Figure 54. Memory Window Measured at Room Temperature and 77K vs. Write/Erase Cycles (N-Channel)

SECTION IX

ENDURANCE

Excessive write/erase cycling can cause window closure, changes in the center voltage, and an increase in the surface state density. Either of these alone, or together, can cause the device to fail. Endurance is the number of write/erase cycles which a device can withstand before it fails. We define endurance here as either the number of cycles needed to make one of the threshold voltages associated with the two memory states equal to the center voltage of the original device before extensive cycling, or the number of cycles at which the threshold window has narrowed to 1V, whichever occurs first. This is illustrated in Fig. 55, which shows the two threshold voltages with write/erase cycling for devices doped with platinum for two oxide thicknesses. It can be seen that, although total window closure may not occur even at 10^6 cycles, the endurance is generally limited to values smaller than this by the excursions of the center voltage. Similar results are observed for n-channel devices. This is seen in Figs. 56 and 57, which show endurance cycling for chromium and iridium doped varactors, respectively.

DEPENDENCE OF ENDURANCE ON WINDOW BEING CYCLED

The endurance of a device which was cycled at relatively low write voltages or short write times, thus giving small windows, was generally not much greater than the endurance for a similar device cycled at high write voltages and times to give large windows. This is illustrated in Fig. 58, in which the window decay of two similar devices is shown for two different original windows. The smaller window was cycled at $\pm$ 30.5V, 1 ms, and the larger one at $\pm$ 35V, 1 ms. The endurance in both cases is seen to be of the order of 1000 cycles, although complete window closure occurs well beyond that.

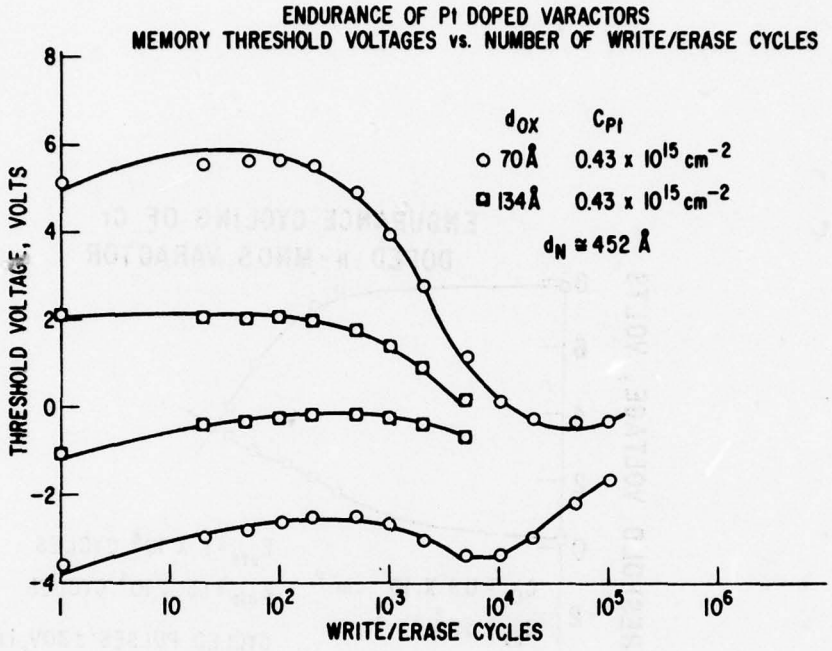


Figure 55. Endurance of Platinum Doped Varactors

(P-Channel)

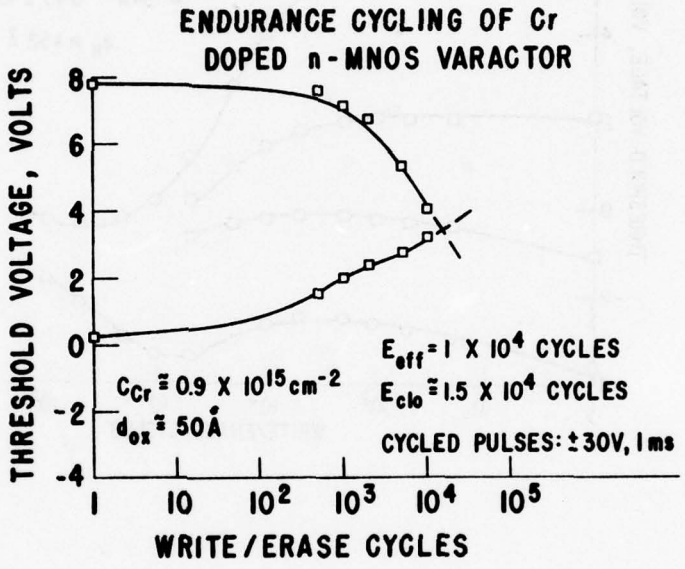


Figure 56. Endurance of Chromium Doped N-Channel Varactors

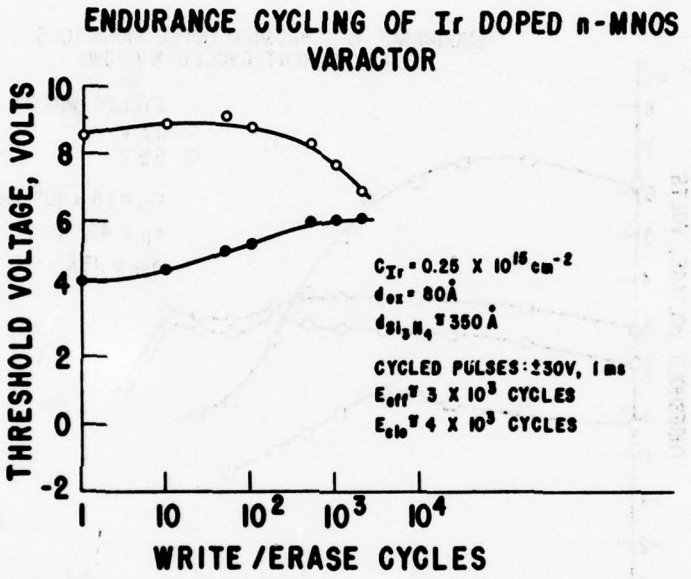


Figure 57. Endurance of Iridium Doped N-Channel Varactors

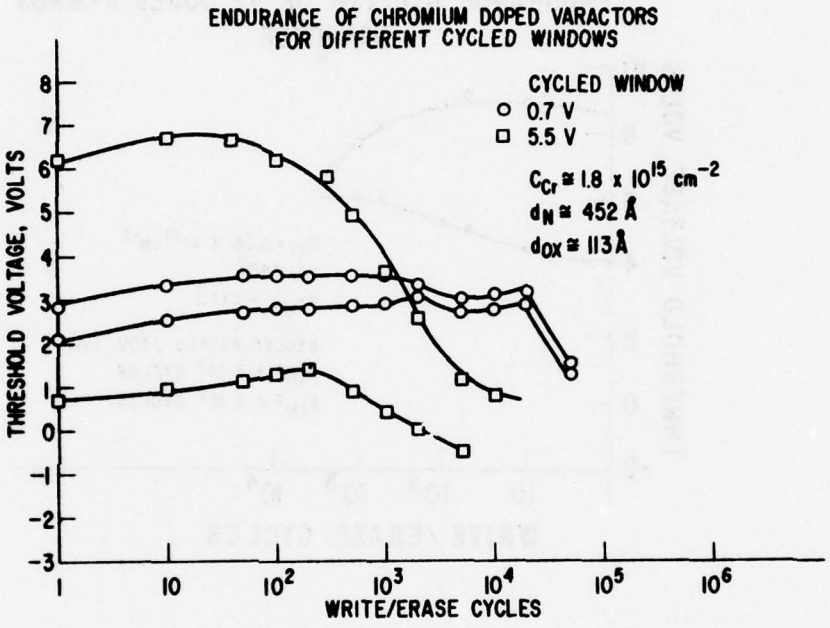


Figure 58. Endurance of Cr Doped Varactors for Different Cycled Windows (P-Channel)

If a device which has been previously cycled to its endurance limit using a low write voltage and a small window, is now cycled again but with a higher voltage, the previous endurance cycling affects the new endurance proportionally. Thus, if at first a 1V window is cycled, and then a 10V window, the second endurance test is hardly affected by the first. Conversely, if a device is cycled with small write voltage, but is then rewritten once with a high write voltage, the endurance appears to be much greater for the smaller windows being cycled. This is illustrated in Fig. 59 in which 4 similar (neighboring) devices were cycled using a 3.5V window ($\pm$ 30V, 1ms), 5.75 V window ($\pm$ 30V, 10 ms), 8V ($\pm$ 35V, 1ms), and 8.25V ($\pm$35V, 10 ms), respectively. The points in Fig. 43 were obtained by cycling to a given number of cycles using the write voltages and times indicated, but then rewriting at the end of this with a $\pm$ 35V, 10 ms write pulse. The less rapid decay of the window at lower write voltages indicates a smaller wear-out effect.

DEPENDENCE OF ENDURANCE ON OXIDE THICKNESS

The dependence of the endurance on the oxide thickness is quite small, and the measured endurances of devices at the same dopant concentration are all the same within about one half decade. This is illustrated in Fig. 60, in which the two memory states of varactors doped with chromium at $C_{Cr} = 1.83 \cdot 10^{15}$ cm^{-2} are plotted as a function of write/erase cycling for six oxide thicknesses (nitride thickness = 452 A). It is seen that the endurance, using the above definition, is from 1000 to about 10,000 cycles, although complete window closure occurs only at about 10^5 cycles. The oxide thickness dependence of the endurance is also small for n-channel devices. This is illustrated in Fig. 61 for a Pt doped varactor. No clear thickness dependence is evident, except that the thinnest oxides generally display a slightly higher endurance.

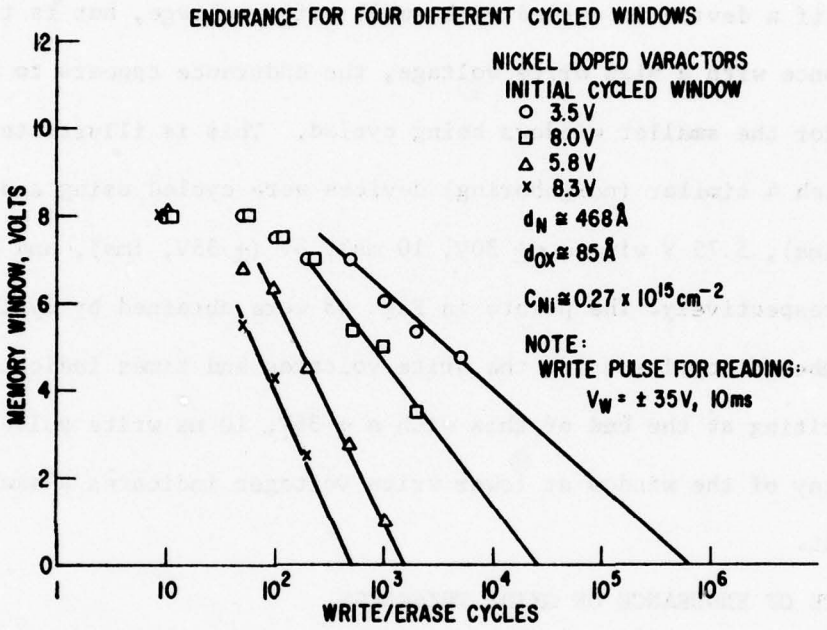


Figure 59. Endurance of Ni Doped Varactors for Four Cycled Windows (P-Channel)

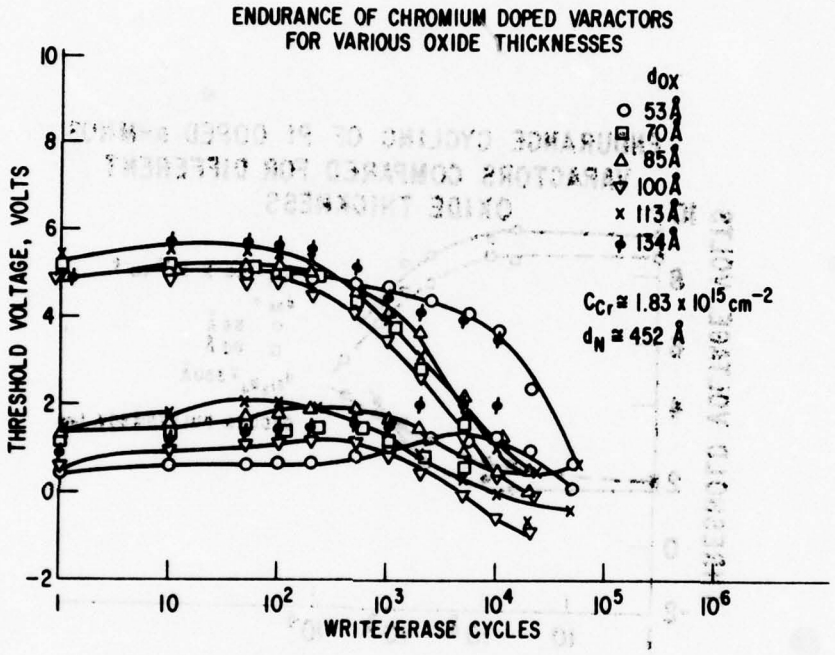


Figure 60. Endurance of Cr Doped Varactors for Various Oxide Thicknesses (P-Channel)

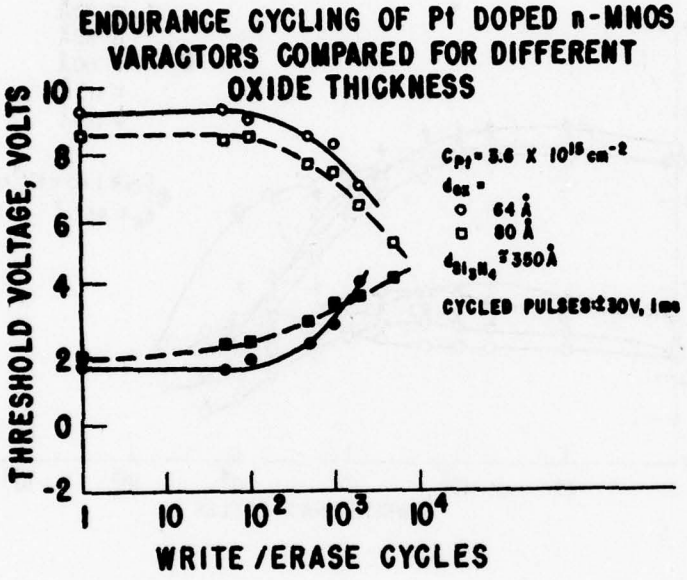


Figure 61. Endurance of Pt Doped N-Channel Varactors for Various Oxide Thicknesses

DEPENDENCE OF ENDURANCE ON DOPANT CONCENTRATION

The dependence on dopant concentration is somewhat more complicated, although even here the dependence is not strong. This dependency is illustrated in Fig. 62 for chromium doped p-channel varactors which have an oxide thickness of 113A and a dopant concentration range of 1.8 to $7.7 \cdot 10^{15}$ cm^{-2}. The endurance levels are the same within about 1 order of magnitude. However, it can be seen that there is an optimum concentration at $3.3 \cdot 10^{15}$ cm^{-2} at which the endurance appears to be a maximum. This maximum is accentuated by plotting the center voltage as a function of dopant concentration after an increasing number of write/erase cycles in Fig. 63. It should be noted that at this concentration very favorable write characteristics and retention are also observed.

Figure 64 shows the endurance of the memory window with write/erase cycling in a Pt doped n-channel device for two different dopant concentrations, but the same oxide thickness. Here also the concentration of 3.6×10^{15} cm^{-2} displays a higher endurance than the lower value of $0.8 \cdot 10^{15}$ cm^{-2}.

TEMPERATURE DEPENDENCE OF ENDURANCE CYCLING

In conventional MNOS devices, the endurance is smaller if the device is write/erase cycled at higher temperatures[5]. In contrast, it was found that the endurance of interface doped MNOS devices is not strongly temperature dependent. This is illustrated in Fig. 65 where the two memory states are plotted as a function of write/erase cycling for various temperatures between room temperature and 200°C. While the threshold voltage decay with cycling is not identical for each temperature, it can be seen that there is no clear temperature dependence of the endurance in the range of these experiments.

---

[5] C. A. Neugebauer and J. F. Burgess, Journal of Applied Physics, Vol. 47, 1976, p. 3182.

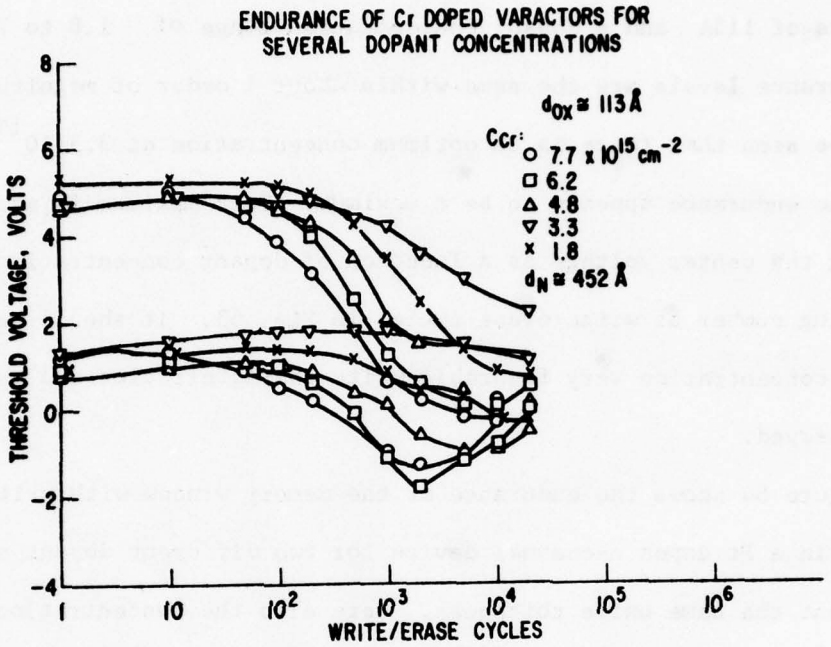


Figure 62. Endurance of Cr Doped P-Channel Varactors for Several Dopant Concentrations

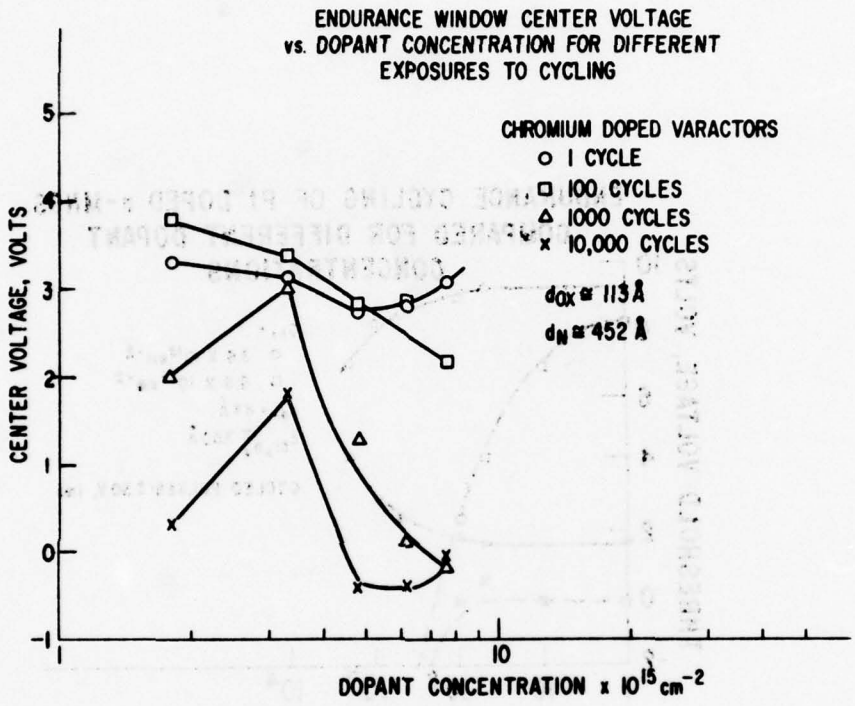


Figure 63. Endurance Window Center Voltage vs. Dopant Concentration (P-Channel)

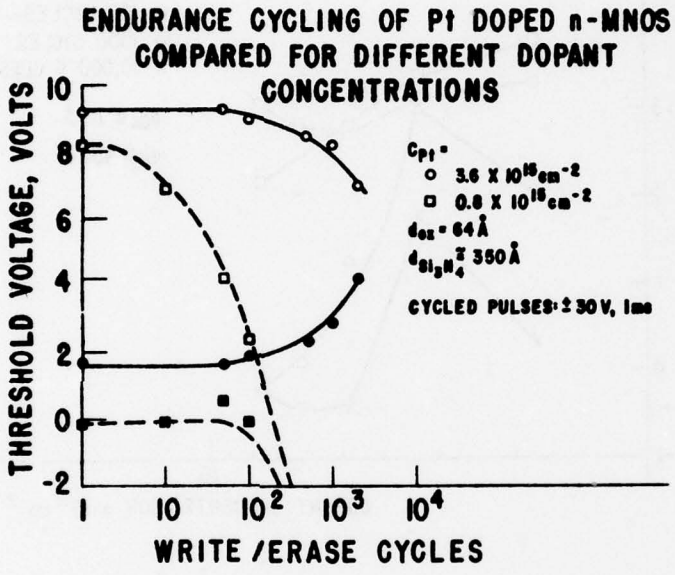


Figure 64. Endurance of Pt Doped N-Channel Varactors for Two Dopant Concentrations

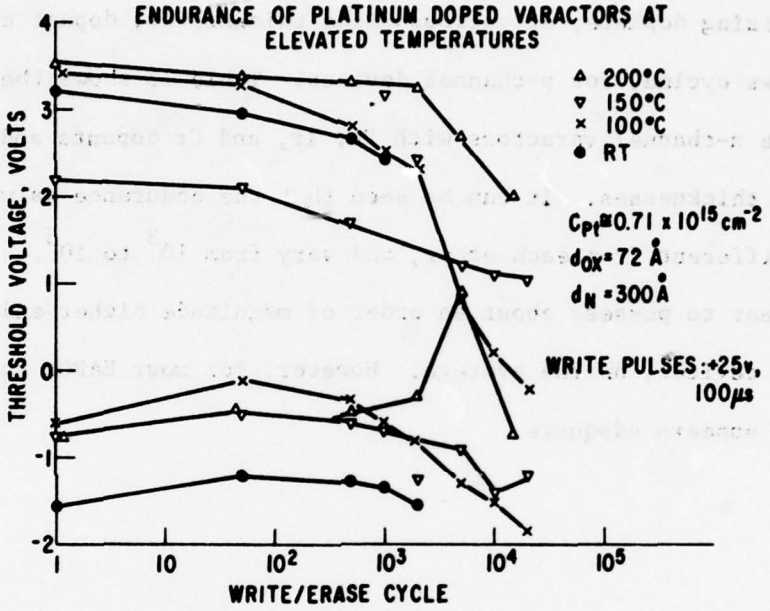


Figure 65. Endurance of Platinum Doped Varactors at Elevated Temperatures, P-Channel Varactors

ENDURANCE OF DEVICES DOPED BY SPUTTERING

Figure 66 illustrates the endurance of a chromium doped device where the dopant was deposited by sputtering. It is apparent that the behavior closely parallels that of evaporation-doped devices.

COMPARISON OF ENDURANCE FOR VARIOUS DOPANTS

Table 12 shows the endurance for varactors and transistors for the six most promising dopants, at various oxide thicknesses, dopant concentrations, and windows cycled, for p-channel devices. Table 13 shows the endurance for comparable n-channel varactors with Pt, Ir, and Cr dopants and 64 and 80A oxide thicknesses. It can be seen that the endurance values are not greatly different from each other, and vary from 10^3 to 10^5. P-channel devices appear to possess about an order of magnitude higher endurance than n-channel devices, on the average. However, for most EAROM applications, the endurance appears adequate.

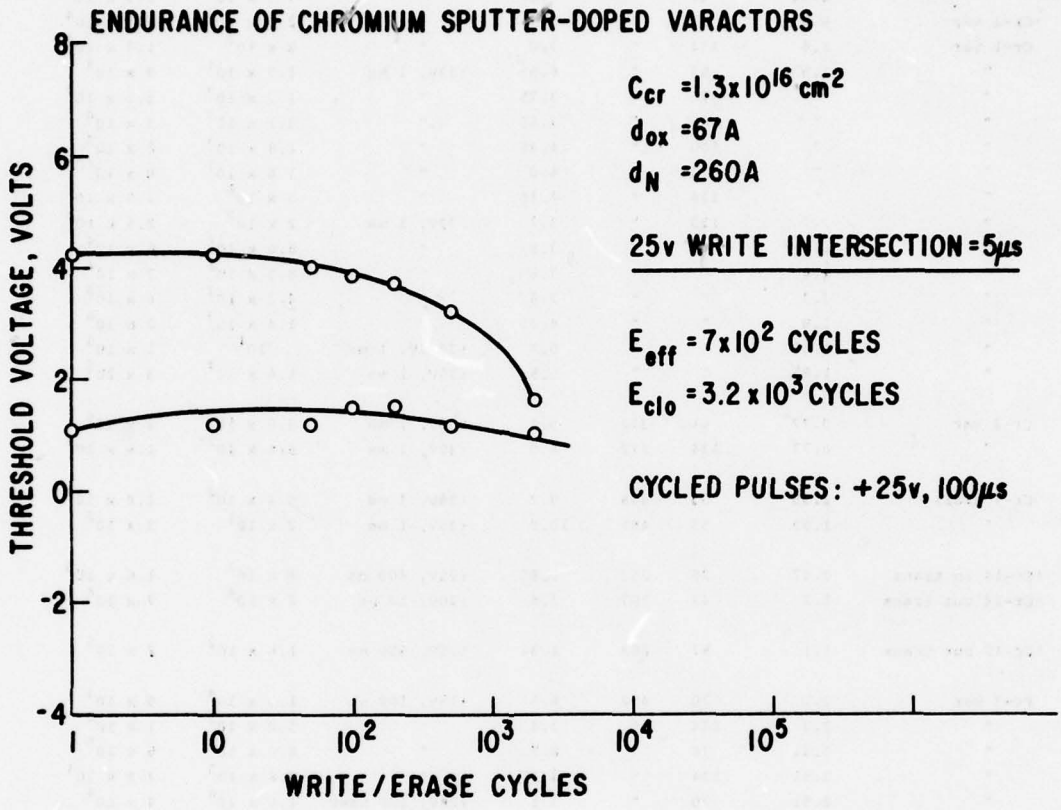


Figure 66. Endurance of Cr Sputter-Doped Varactors

TABLE 12

ENDURANCE PARAMETERS FOR P-CHANNEL DEVICES

Device	Dopant conc. $\times 10^{15}$ cm^{-2}	d_{ox} Å	d_N Å	Window cycled V	Pulse dimensions	Effective endurance	closure (est.)
Cr-1 var	2.95	134	452	3.05	±35V, 100 µs	6×10^2	7×10^4
"	2.95	53	"	3.17	"	7.5×10^4	2.5×10^5
†Cr-1 var	8.6	53	"	5.7	"	2.5×10^3	1.5×10^4
Cr-1 var	8.6	134	"	3.0	"	8×10^2	1.5×10^4
"	1.83	53	"	4.55	±33V, 1 ms	1.7×10^4	9×10^4
"	"	70	"	3.75	"	1.7×10^3	1.5×10^4
"	"	85	"	3.65	"	3.1×10^3	5×10^4
"	"	100	"	4.35	"	1.8×10^3	2×10^5
"	"	113	"	4.0	"	1.6×10^3	8×10^4
"	"	134	"	4.15	"	$\sim 5 \times 10^4$	1.5×10^5
"	7.7	113	"	3.7	±32V, 1 ms	2×10^2	2.5×10^4
"	6.2	"	"	3.8	"	5.0×10^2	6×10^4
"	4.8	"	"	3.8	"	8.0×10^2	7×10^4
"	3.3	"	"	3.4	"	4.3×10^3	6×10^5
"	1.8	"	"	4.35	"	1.4×10^3	2×10^6
"	1.85	"	"	0.7	±30.5V, 1 ms	10^1	1×10^5
"	1.85	"	"	5.5	±35V, 1 ms	1.4×10^3	3×10^5
Cr-2 var	0.77	61	372	5.5	±30V, 1 ms	$3.0 \times 10^{3*}$	2×10^4
"	0.77	134	372	4.9	±30V, 1 ms	$6.6 \times 10^{2*}$	1.6×10^3
Cr-7 trans	1.95	53	468	9.2	±30V, 1 ms	6.4×10^2	1.5×10^4
"	1.95	53	468	10.8	±35V, 1 ms	2×10^1	3×10^2
†Cr-14 in trans	2.47	35	263	3.85	±25V, 400 ns	4×10^3	1.6×10^5
†Cr-14 out trans	5.2	43	263	3.6	±20V, 10 µs	2×10^4	7×10^6
†Cr-15 out trans	1.1	57	263	1.34	±25V, 500 ns	1.6×10^2	2×10^5
Pt-7 var	2.3	70	452	8.5	±35V, 100 µs	1.3×10^4	9×10^4
"	2.3	134	"	3.4	"	3.0×10^3	1×10^4
"	0.51	70	"	8.7	"	6.0×10^3	6×10^5
"	0.51	134	"	3.2	"	3.6×10^3	2.5×10^4
"	0.51	70	"	3.1	±28V, 100 µsec	1.0×10^4	4×10^4
"	0.51	70	"	5.3	±25V, 10 ms	1.1×10^4	8×10^5
"	0.51	70	"	2.8	±35V, 1.75 µs	1.6×10^2	4×10^4
"	0.51	70	"	6.8	±35V, 10 µs	$5.2 \times 10^{4*}$	6×10^7
†Pt-11 trans	1.12	85	372	2.3	±25V, 100 µs	1.5×10^3	6×10^4
† "	0.27	85	"	4.6	±25V, 1 ms	4×10^1	2.0×10^4
W-17 var	1.65	59	468	5.45	±35V, 100 µsec	2.1×10^2	8×10^2
"	0.06	59	"	4.5	"	8.0×10^3	2.3×10^4
W-39 var	0.55	63	450	1.2	±35V, 1 ms	$\sim 10^1$	8×10^4
"	2.5	63	"	2.0	±35V, 1 ms	$>1.4 \times 10^4$	-
W-44 in var	1.08	68	439	10.2	±35V, 1 ms	-	1.1×10^3
"	"	100	"	7.6	"	-	5×10^3
W-44 out var	"	68	"	8.1	"	-	2×10^4
"	"	100	"	5.0	"	-	3.2×10^7
W-45 in var	2.8	68	"	8.2	"	4.0×10^3	4×10^4
W-45 out var	"	68	"	7.1	"	-	7×10^4
"	"	100	"	4.2	"	-	3.5×10^5
W-45 in var	2.8	68	"	6.35	±35V, 1 ms	6.0×10^3	1.4×10^6

TABLE 12 Concluded

Device	Dopant conc. $\times 10^{15}$ cm^{-2}	d_{ox} Å	D_N Å	Window cycled	Pulse dimensions	Effective endurance	Window closure (est.)
W-44 in var	1.08	68	439	8.4	±35V, 1 ms	4.0×10^2	2×10^3
W-47 trans	1.79	84	280	5.6	±25V, 1 ms	1.0×10^3	2.3×10^4
†W-47 var	1.79	84	280	4.3	"	2.0×10^3	1.6×10^4
W-48 var	1.94	58	320	5.5	±30V, 10μs	1.1×10^4	8.4×10^4
Ir-2 var	0.081	53	468	6.5	±35V, 1 ms	3.2×10^3	5.5×10^3
"	0.081	80	"	5.8	±32.5V, 1 ms	$1.3 \times 10^{3*}$	2×10^4
"	0.081	85	"	6.6	±35V, 1 ms	1.1×10^3	3.6×10^3
"	1.09	80	"	6.6	±30V, 1 ms	$>10^5$	7×10^5
Ni-4 var	1.22	53	468	4.9	±30V, 1 ms	$>2.0 \times 10^{4*}$	6×10^6
"	0.27	85	"	6.9	"	$>1.0 \times 10^{4*}$	1×10^5
"	1.22	53	"	7.75	±35V, 1 ms	3.5×10^4	1.6×10^4
"	"	"	"	4.0	±30V, 1 ms	$6.0 \times 10^{6*}$	5×10^6
"	"	"	"	7.0	±30V, 10 ms	$1.0 \times 10^{5*}$	1.1×10^5
"	1.22	"	"	9.2	±35V, 10 ms	$1.5 \times 10^{3*}$	1×10^4
"	0.27	85	"	3.5	±30V, 1 ms	-	7×10^5
"	"	"	"	8.0	±35V, 1 ms	-	1.6×10^3
"	"	"	"	5.8	±30V, 10 ms	-	2.5×10^4
"	"	"	"	8.3	±35V, 10 ms	-	5×10^2
Ni-10 var	0.39	58	320	6.2	±30V, 10 μs	3.1×10^2	2.3×10^3
Pt-16 var	0.12	58	320	5.2	±30V, 10 μs	2.1×10^2	4.8×10^2
Pd-3 tr	0.86	85	372	4.7	±25V, 100μs	3.6×10^2	2×10^4
"	1.58	85	372	5.2	±25V, 1 ms	2.2×10^1	7×10^3
Cr-4 tr	0.81	85	372	3.0	±25V, 1 ms	1.6×10^2	4×10^2
"	3.9	"	"	5.2	±25V, 1 ms	-	6×10^1
"	3.9	"	"	3.95	±25V, 100 μs	5.7×10^2	1.7×10^3
Pt-4 var	0.17	65	564	4.9	±35V, 1 ms	4.5×10^3	4.5×10^3
"	1.55	"	"	4.5	" "	6.6×10^3	1.0×10^4
"	2.76	"	"	4.3	" "	3.8×10^3	6.0×10^3
W-38 var	1.01	65*	~590	5.7	" "	7.6×10^2	2.5×10^3
Ir-7 var	0.15	58	320	5.5	±30V, μs	5.6×10^2	1.8×10^3

†These devices could qualify as fast write devices.

*These devices were cycled with pulses of different dimension from those used to write the threshold voltages we actually measured. In all cases, pulse of 35V, 1 ms was used to write the actually observed window.

NOTE:
Effective endurance of a device is defined as that number of write-erase cycles that a device can accommodate before one of the threshold voltages intersects the original center voltage.

TABLE 13

ENDURANCE PARAMETERS FOR N-CHANNEL DEVICES

Dopant	Dopant Conc. $x10^{15}$ cm^{-2}	d_{ox} Å	d_{Nit} Å	Window Cycled V	Pulse Dimensions	Effective Endurance	Window Closure (est)
Platinum	3.6	64	~ 350	7.5	±30V, 1ms	$5x10^3$	$5x10^3$
	0.83	"	"	8.4	"	60	$1x10^3$
	0.83	80	"	7.7	"	40	$2x10^3$
	3.6	"	"	6.5	"	$5x10^3$	$8x10^3$
	2.7	85	312	9.6	±35V, 100μs	$1.5x10^2$	$3x10^3$
Iridium	1.1	80	~ 350	2.4	±30V, 1ms	6	
	0.25	"	"	4.1	"	$3x10^3$	$4x10^3$
	"	64	"	3.8	"	80	$5x10^4$
Chromium	1.1	50		6.4	±30V, 1ms	$1 x10^4$	$2 x10^5$
	4.1	85	312	7.4	±35V, 100μa	$2.2x10^2$	$2 x10^3$
	0.9	~ 50		7.6	±30V, 1ms	$1 x10^4$	$1.5x10^4$

SECTION X

TOTAL DOSE IONIZING RADIATION EFFECTS IN INTERFACED DOPED MNOS TRANSISTORS

INTRODUCTION

In this section the behavior of interface doped memory transistors under total dose ionizing radiation is described. Included is a comparison to undoped devices, effect of various dopants, interface dopant concentration dependence, gate bias effects, oxide thickness effects, ability to re-write and memory retention after irradiation. Also described is the radiation behavior of stable gate interface doped transistors at various gate biases, dopants, and doping levels. Both p- and n-channel memory transistors were tested, while the results on stable gate transistors are reported for p-channel devices only.

Preliminary evaluation of 16 p-channel interface doped MNOS devices was carried out in the on-site electron accelerator facility. Ionizing radiation was provided by a 1.5 MeV electron beam produced in a high voltage electron accelerator of the resonant transformer type. The beam is on intermittantly at a rate of 180 Hz and a 10% duty cycle. Calibration was in terms of rads (Si) using a standard 15 millicurie Co^{60} source and thermoluminescent CaF_2:MnO radiation dosimeters obtained from Harshaw Chemical, in conjunction with Harshaw model 2000A and B thermoluminescence detectors. The average dose rate delivered by the beam can be varied between 10^3 and 10^8 rads (Si)/sec. The total dose level was increased by increasing the time of exposure. Exposure to the beam took place with the package lids removed. Five volts was the magnitude of drain bias voltages in these and subsequent tests.

Both stable gate and memory p-channel transistors were irradiated to a maximum total dose of 2×10^7 rads (Si). Stable gate devices were tested under

bias. Positive and negative memory states of Pt, Pd, W, Cr, and Ir doped transistors were exposed. Results from these experiments dictated the appropriate radiation and bias levels to be used during large scale device testing. It was observed that

- For stable gate devices, significant threshold voltage shift would not occur before a total dose exposure to 10^3 rads (Si).
- Irradiation of stable gate devices under +10V or -10V bias accelerated threshold shift markedly, though at different rates.
- Even under zero bias, stable gate threshold shifts surpassed 10V at a total radiation dose of 10^7 rads (Si).
- Positive memory states are most sensitive to radiation effects.
- Significant memory threshold decay occurs after a total dose of 10^3 rads (Si) and measures over 8V at 10^7 rads (Si).

Final radiation testing was carried out in the Co^{60} radiation facility at the Cambridge Air Force Research *Laboratories* (CRL). A total of approximately 150 transistors were exposed to eight different radiation levels up to $3 \cdot 10^6$ rads (Si). Both stable and memory gates were exposed for p-channel, and memory devices only for n-channel. Dopants investigated were Pt, Pd, W, Ni, Cr, and Ir. Dopant concentrations and gate oxide thickness were varied. Undoped devices were included for comparison. Bias voltages during exposure were 0, $\pm$ 5, and $\pm$ 10V. Thermoluminescent CaF_2:MnO radiation dosimeters were also exposed for calibration. Appendix A contains a comparison of radiation levels recorded by these crystals and those used to calibrate the electron beam source. Results from the Co^{60} gamma radiation testing and the preliminary high energy electron beam experiments indicate that, under the test conditions used in both cases, MNOS device stability is independent of the source.

IRRADIATION OF STABLE GATE P-CHANNEL TRANSISTORS

The p-channel stable gate devices used in these experiments differ from the memory devices only in that the oxide film was over 500Å thick, rather than less than 100Å. The dopant and the nitride are still present. Chromium and iridium doped and undoped devices were tested. Dopant concentrations were varied and a number of gate biases were applied, namely, ±10V, ±5V and 0V. The gate material is aluminum and dopant concentrations ranged between 10^{14} and 10^{16} cm^{-2}.

Comparison with undoped devices

The presence of chromium interface dopant in stable transistors does affect the irradiation hardness. Figure 67 shows the threshold voltage decay curves of an undoped device and chromium and iridium doped devices. In terms of absolute threshold voltage shift, at zero bias the chromium doped device is the most resistant. The iridium doped and undoped devices behave very similarly. In all three cases, threshold shifts of 1V or more do not occur until a total dose radiation level of 10^4 rads (Si) is reached.

Dopant concentration dependence

While experiment indicates that the presence of a metal dopant at the interface can affect device stability, threshold decay was found to be largely independent of dopant concentration within the range studied. This can be seen in Fig. 68 in which the decay curves of four chromium doped transistors are shown. The dopant concentrations vary from 1.9 to 6.3 x 10^{15} cm^{-2}. When the radiation level at which the threshold has shifted 5V was plotted in Fig. 69 as a function of chromium dopant concentration, it appears that, as the chromium concentration increases, the device hardness increases slightly.

Figure 70 contains the decay curves of iridium doped devices at three different dopant concentration levels. These curves, like those in Fig. 69,

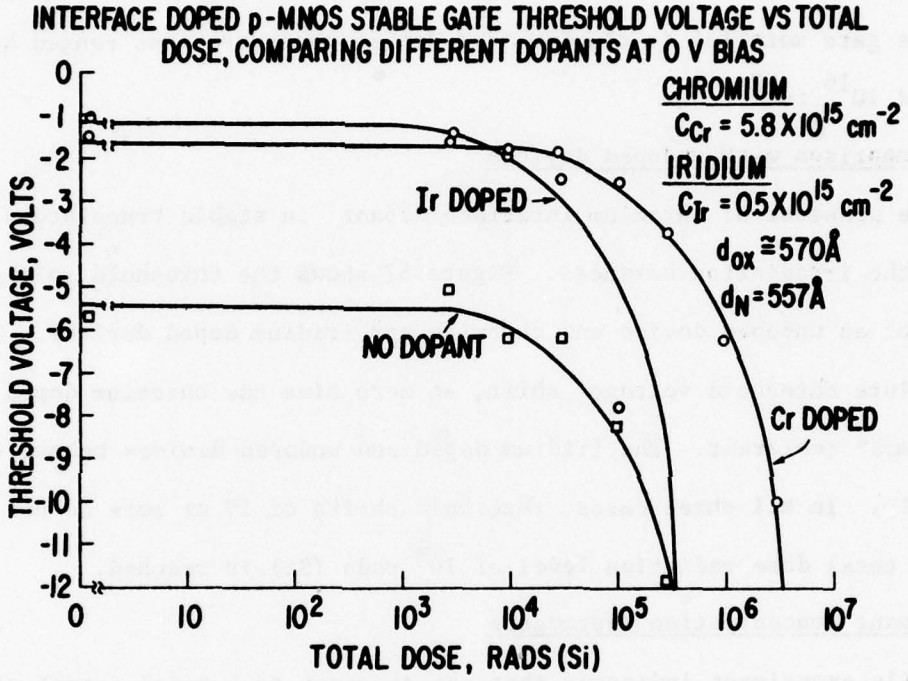


Figure 67. Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Doped Devices Compared to Undoped Device

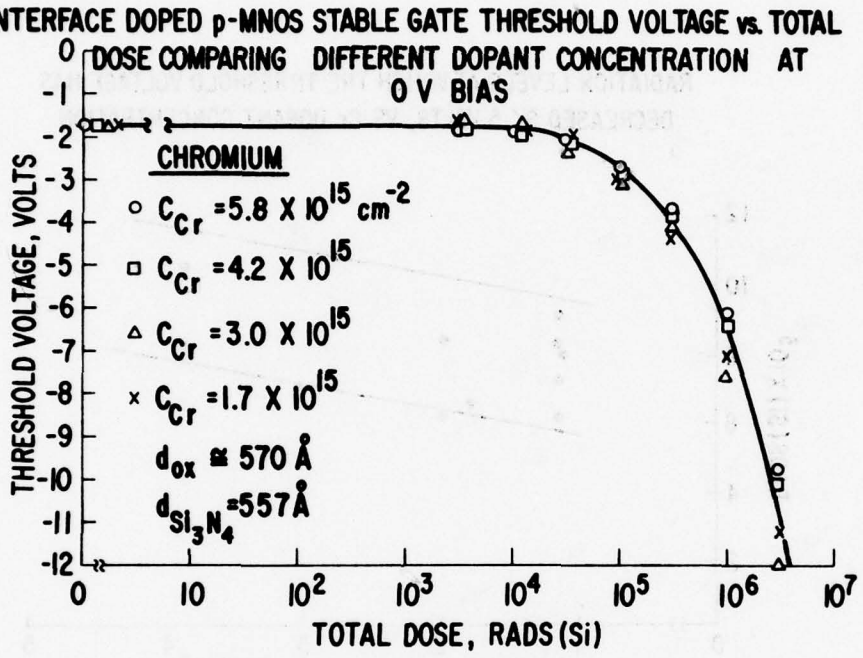


Figure 68. Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Comparing Effects of Different Cr Concentrations

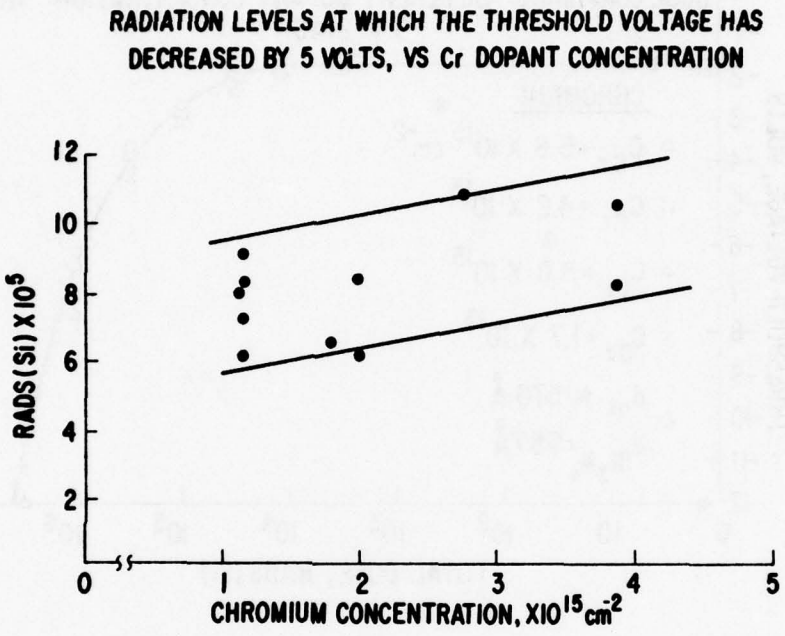


Figure 69. Threshold Shift During Irradiation as a Function of Cr Concentration

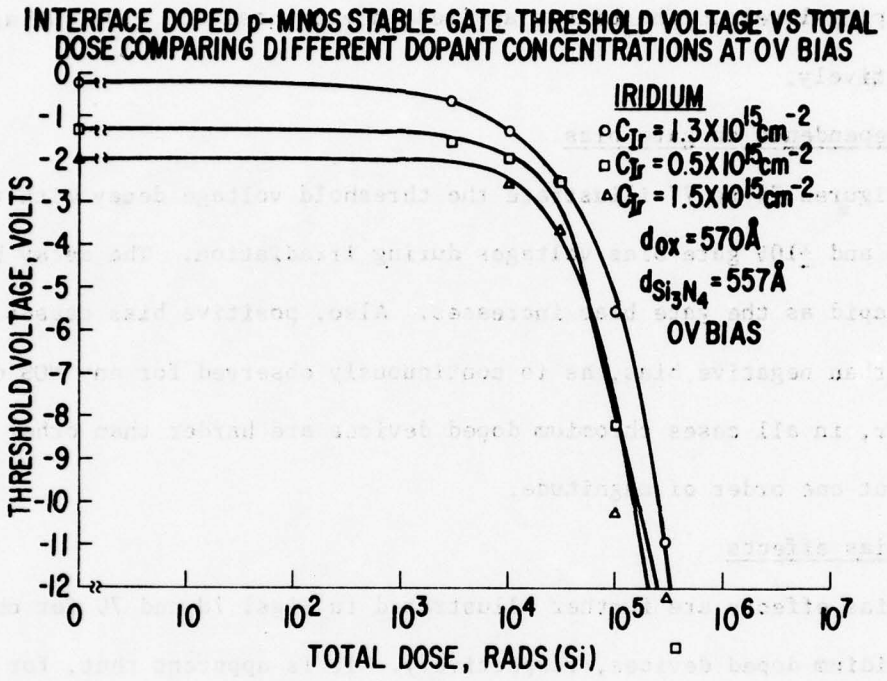


Figure 70. Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Comparing Effects of Different Ir Concentrations

do not suggest more than a second order dependence of radiation hardness on metal dopant concentration.

Even when doped devices are irradiated under a gate bias, the threshold voltage decay remains independent of dopant concentration. Figures 71, 72 and 73 each show the decay curves of two chromium doped devices with different doping levels. The biases applied in each case are +10V, 0V and -10V, respectively.

Dependence on gate bias

Figures 74 to 77 illustrate the threshold voltage decay with total dose for $\pm$5 and $\pm$10V gate bias voltages during irradiation. The decay becomes more rapid as the gate bias increases. Also, positive bias causes faster decay than negative bias, as is continuously observed for any MOS device. However, in all cases chromium doped devices are harder than other dopants by about one order of magnitude.

Bias effects

Bias effects are further illustrated in Figs. 78 and 79 for chromium and iridium doped devices, respectively. It is apparent that, for both dopants, devices with no bias are most radiation resistant and devices with positive applied bias are least resistant. Curiously, at -10V applied gate bias, some devices exhibit an "upturn" as shown by the data points in Fig. 80. This effect was not observed for other gate biases.

Figures 81 and 82 are plots of device gain vs. total dose radiation for chromium and iridium doped transistors with similar dimensions. In the former, the devices were irradiated with gates biased at +10V. In the latter, no gate bias was applied. Application of worst case bias has caused the gain of both devices in Fig. 81 to degrade two orders of magnitude after 10^6 rads (Si) while similar devices irradiated under zero bias experienced gain shifts of less than one order of magnitude.

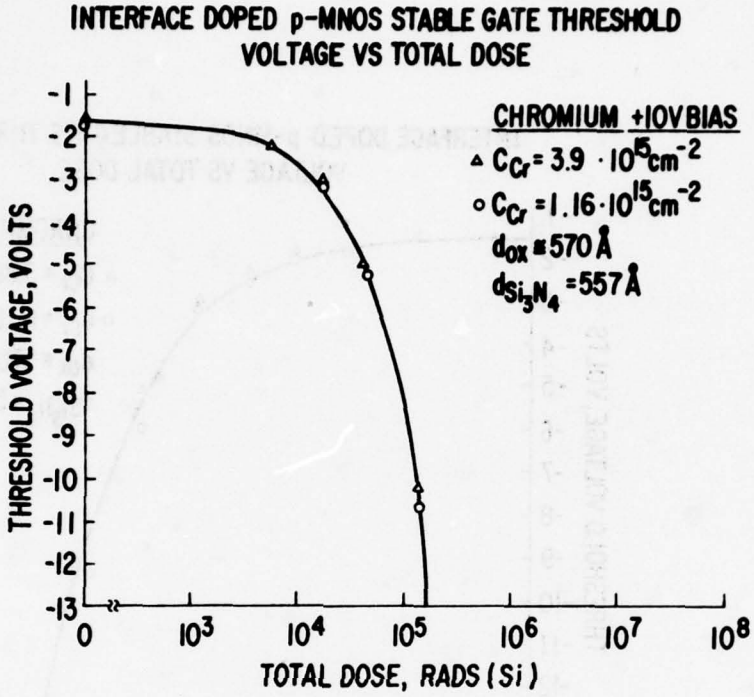


Figure 71. Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Effects of +10V Gate Bias on Two Cr Concentrations

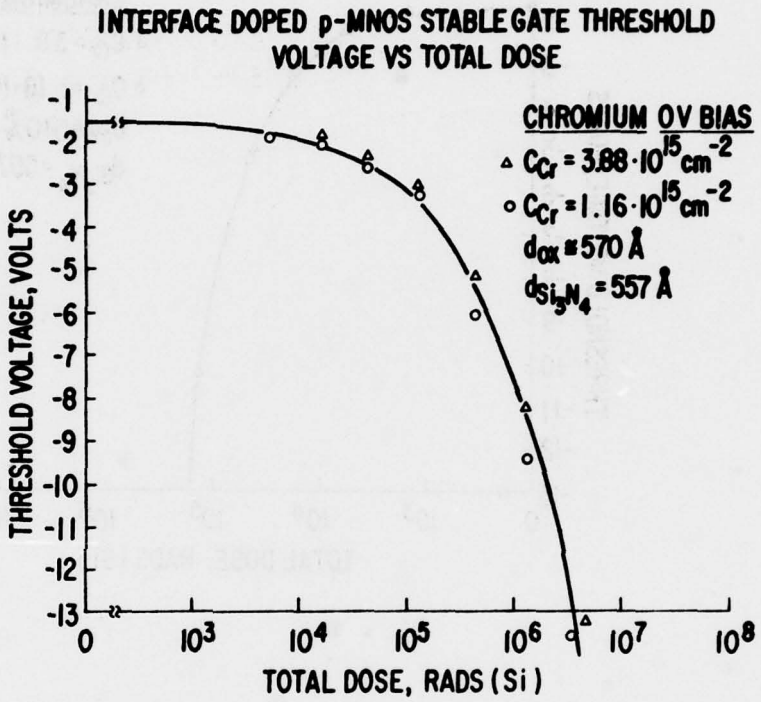


Figure 72. Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Effects of 0V Gate Bias on Two Cr Concentrations

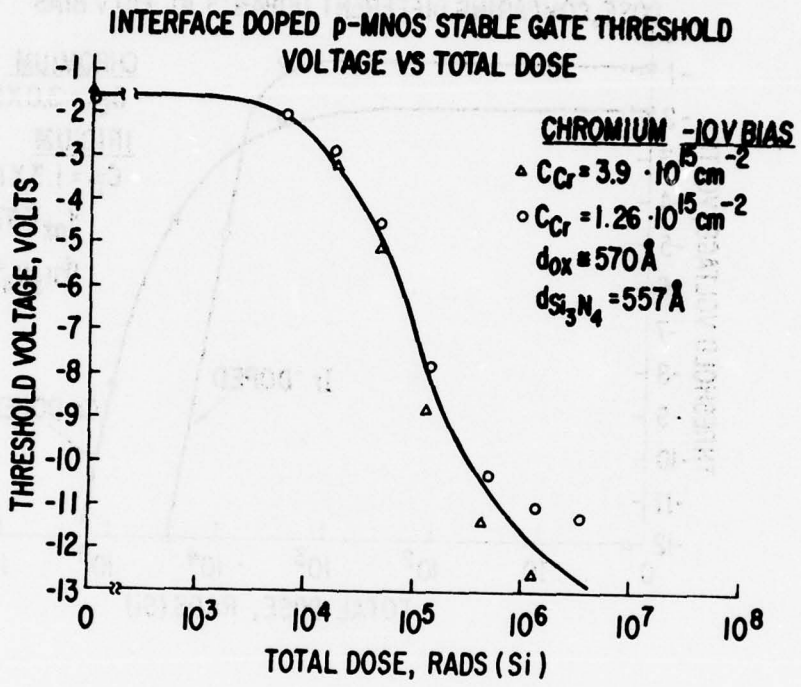


Figure 73. Stable Gate P-Channel Threshold Voltage vs. Total Dose Radiation, Effects of -10V Gate Bias on Two Cr Concentrations

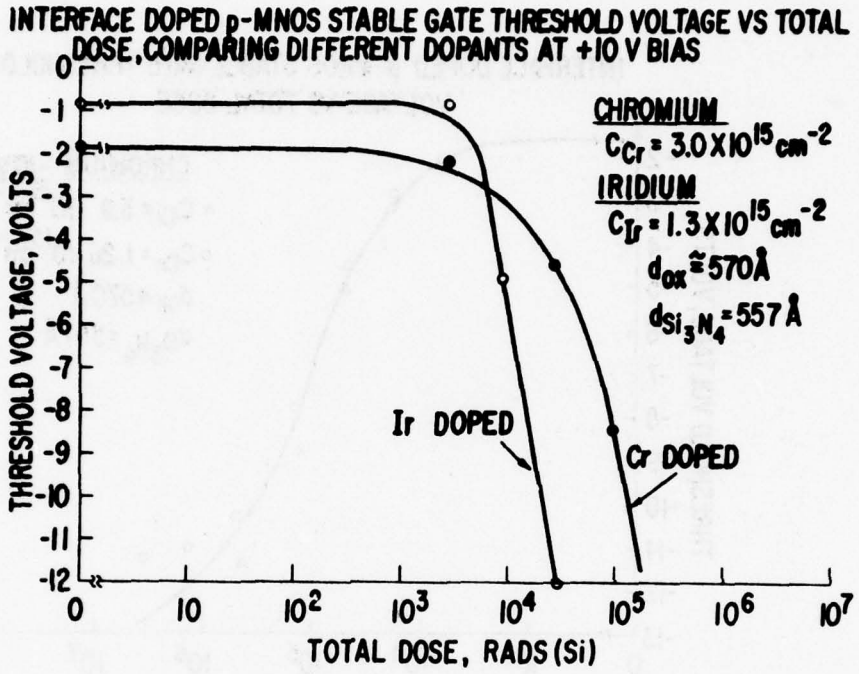


Figure 74. 10V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation

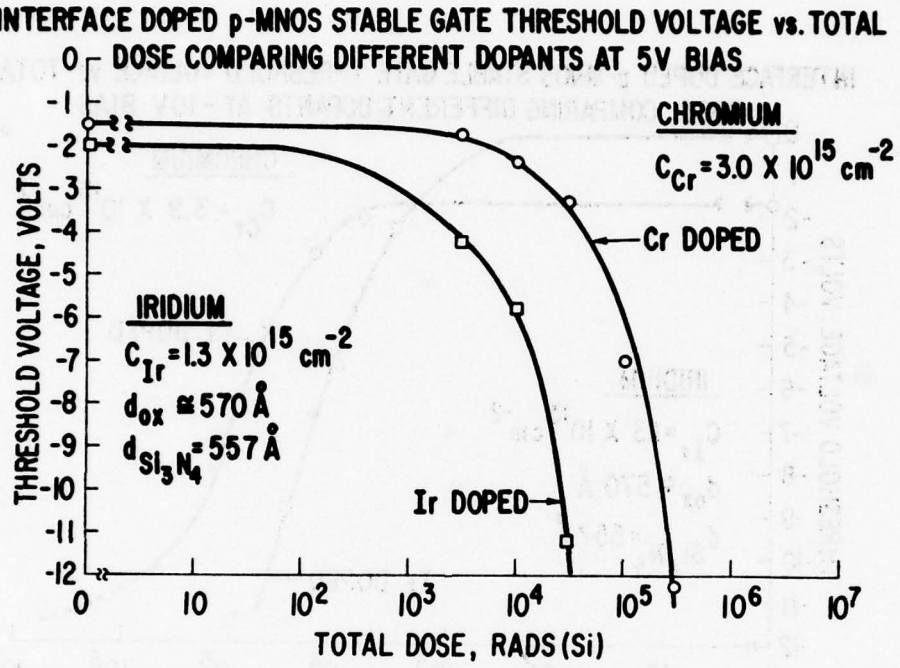


Figure 75. 5V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation

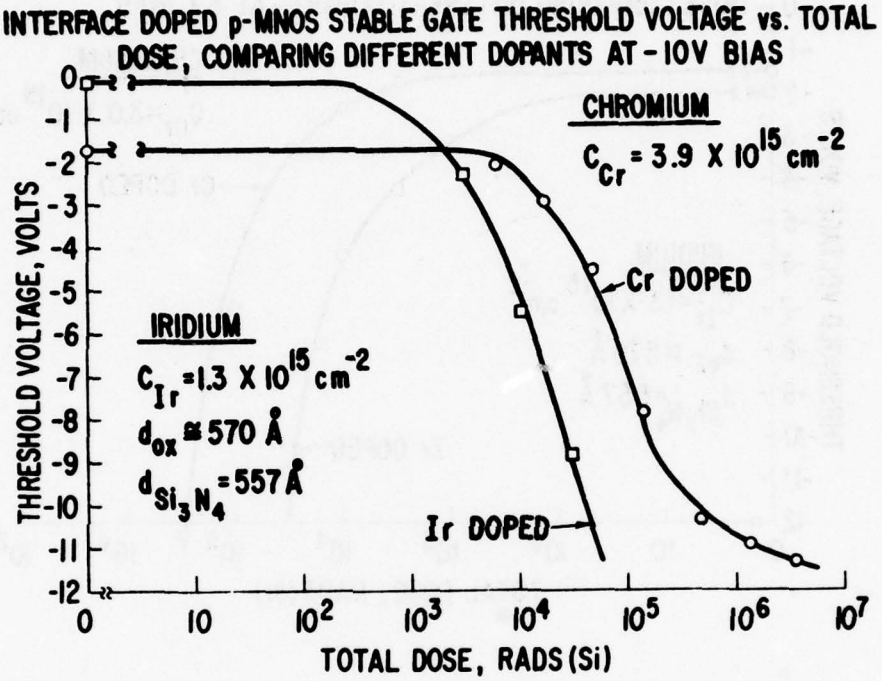


Figure 76. -10V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation

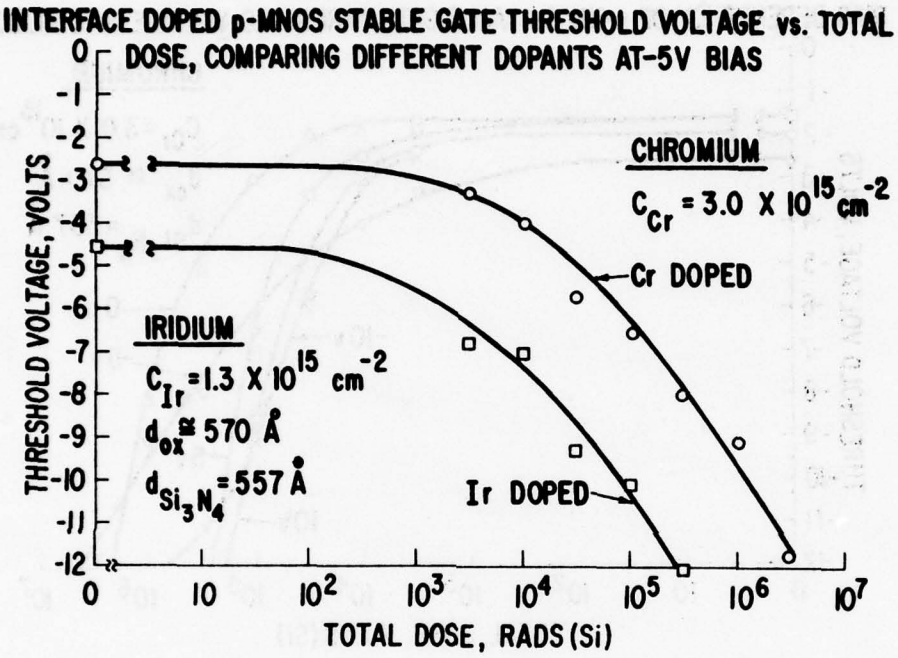


Figure 77. -5V Gate Bias Applied to Cr and Ir Doped Stable Gate P-Channel Transistors During Irradiation

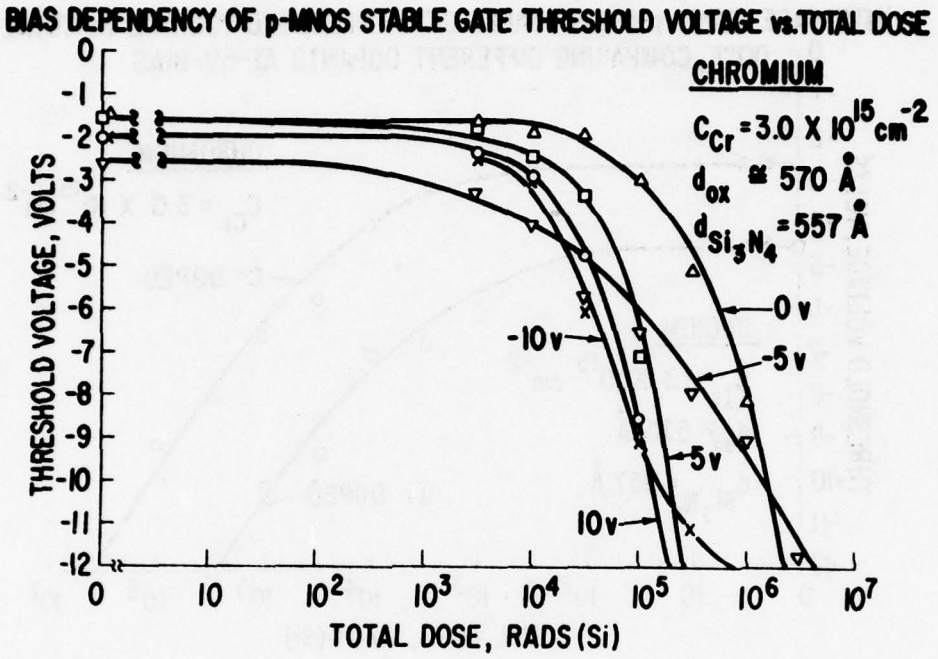


Figure 78. Bias Effects in Cr Doped P-Channel Stable Gate Transistors During Irradiation

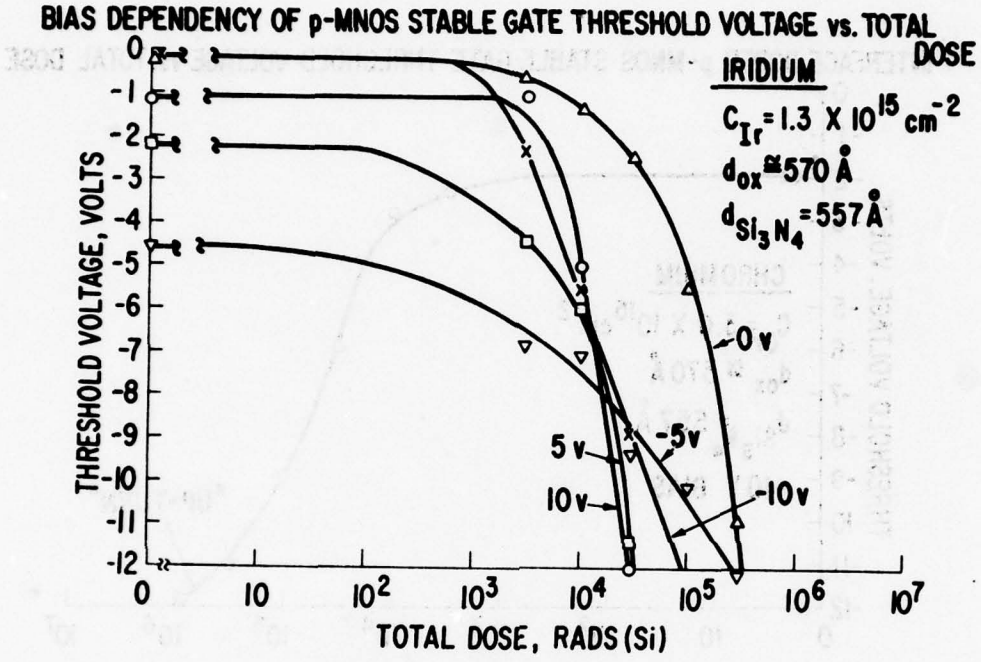


Figure 79. Gate Bias Effects in Stable Gate Ir Doped P-Channel Transistors During Irradiation

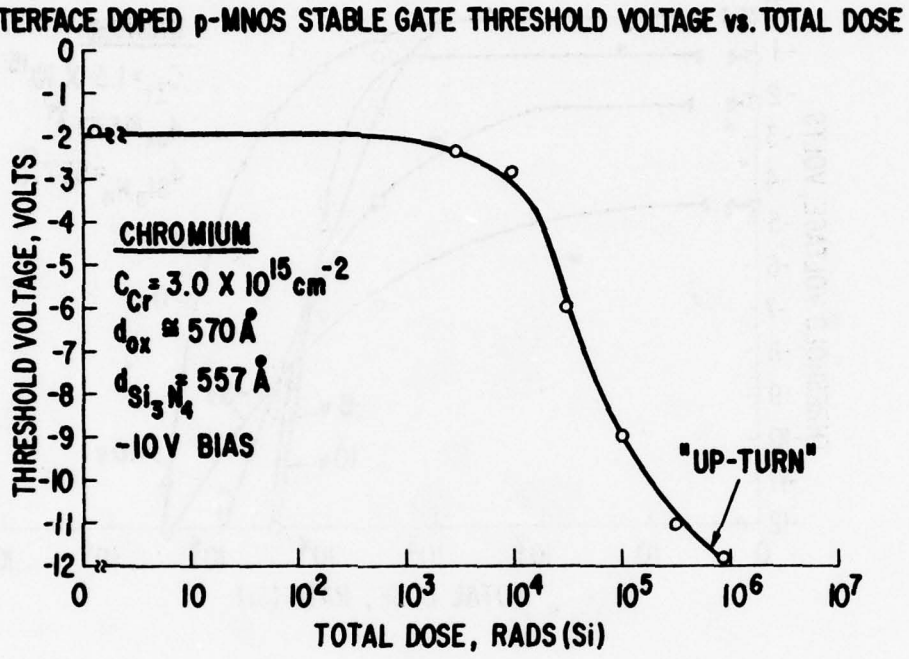


Figure 80. Stable Gate Threshold "Upturn" During Irradiation with Negative Gate Bias

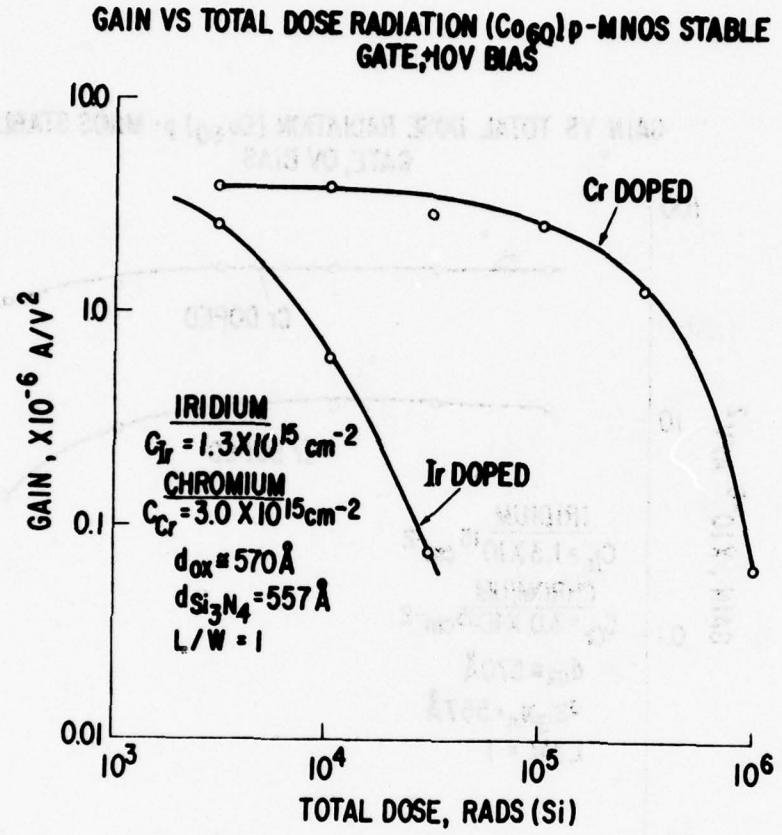


Figure 81. Irradiated Stable Gate Transistor Gain, Positive Gate Bias

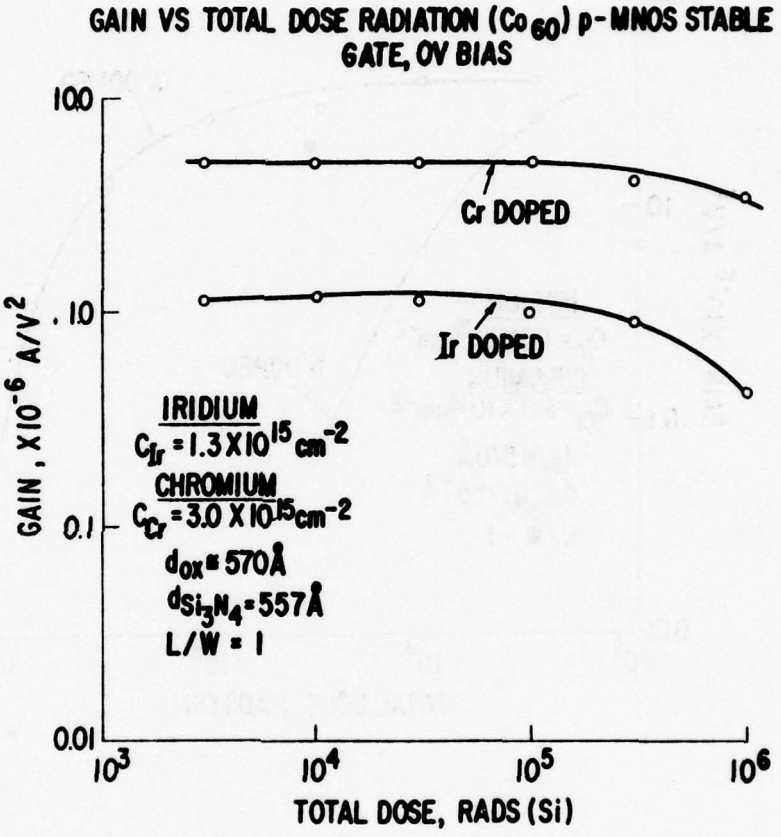


Figure 82. P-Channel Stable Gate Transistor Gain with Zero Bias During Irradiation

IRRADIATION OF MEMORY TRANSISTORS

Ionizing radiation can have drastic effects on the properties of MNOS memory devices. First, the memory window may shrink or close entirely. Second, the position of the center voltage may change. Third, gate shorts may appear. Fourth, the retention may decrease, and fifth, the device may be only partially rewritable.

Previous work at this Laboratory on conventional, undoped, thin oxide (20A) MNOS memory devices has indicated that exposure levels less than 10^7 rads (Si) did not result in appreciable changes in the memory window; however, the center voltage begins to change above 10^5 rads (Si). Gate shorts appeared at levels above 10^8 rads. Retention was not affected by radiation up to 10^7 rads (Si), for these devices.

In the present experiments, both p-channel and n-channel aluminum gate interface doped memory transistors were tested. The oxide thickness of most devices was 85Å. Some 57Å oxide devices were included for comparison. The dopants were chromium, platinum, iridium, tungsten, nickel and palladium, the six most promising dopants. The doping levels fall between 10^{14} and 10^{15} cm^{-2}. The nitride thickness was 370Å in most cases. Positive and negative memory states were written into these devices several days in advance of irradiation. This was possible because of the high retention properties of these devices. Gate biases of +10V, $\pm$ 5V and 0V were applied during irradiation.

Comparison with undoped devices

Figure 83 shows the decay with increasing total dose of high and low threshold states for an undoped MNOS memory transistor under zero bias. It should be noted at this point that an undoped MNOS device with 85Å oxide

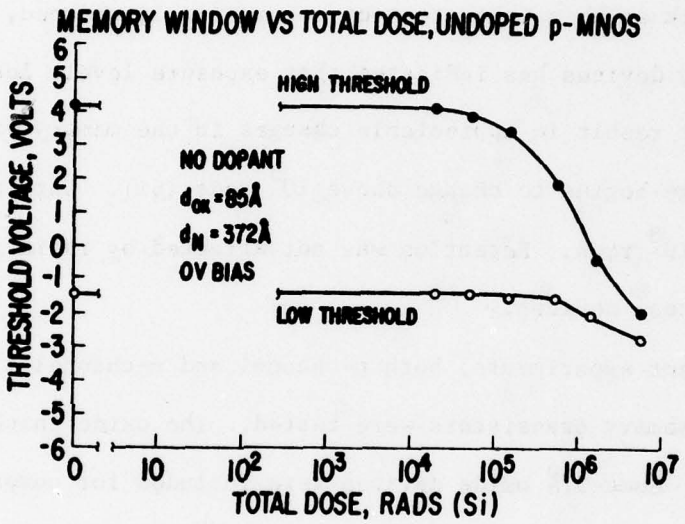


Figure 83. P-Channel Memory Window vs. Total Dose Radiation for Undoped P-Channel Transistors

thickness is not generally useful because of its inability to eject the negative charge stored at the oxide-nitride interface which is associated with the high threshold voltage. This device was, therefore, tested only to ascertain the effect of doping the interface on the total dose behavior. The high threshold was achieved through normal writing procedures. However, since it isn't possible to eject stored charge from the interface of an undoped device, an unwritten threshold state was irradiated to simulate the negatively written state.

For the undoped devices, the more positive thresholds show initial signs of decay between 10^4 and 10^5 rads (Si) - very much like the interface doped stable gate devices. The more negative threshold state begins to decay at a much higher radiation level, namely, ten times greater than in the more positive state and its total shift at $3x10^6$ rads (Si) is only 30% of the positive threshold shift.

Similar results are observed at zero bias for iridium, tungsten, platinum, palladium, nickel and chromium doped p-channel and platinum doped n-channel devices as shown in Figs. 84 through 90. In all cases, the memory window begins to shrink after a total dose of 10^4 to 10^5 rads (Si). The shrinkage is due primarily to the decay of the positive threshold which is also responsible for a change in the center voltage of the memory windows that is dependent on the total dose.

Since it is the positive threshold decay which almost entirely determines the radiation resistance of a device, the effect of using different dopants can be demonstrated in Fig. 91 where the decay curves of positive thresholds for several dopants are compared.

When absolute threshold shifts are measured, no dopant provides a significantly higher hardness level over the others.

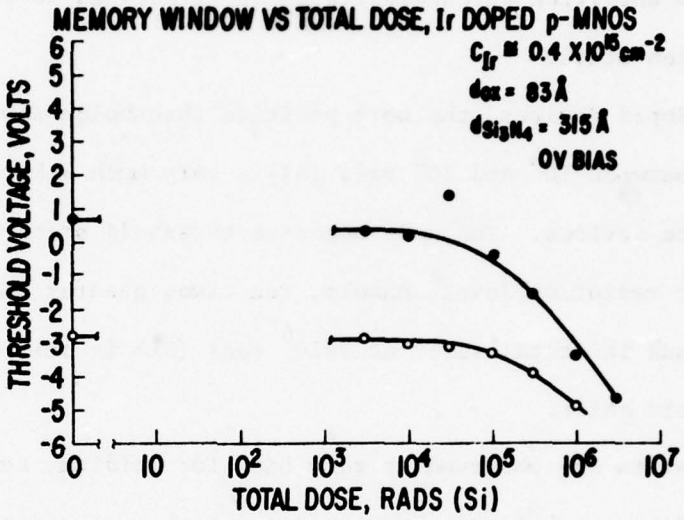


Figure 84. Ir Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias

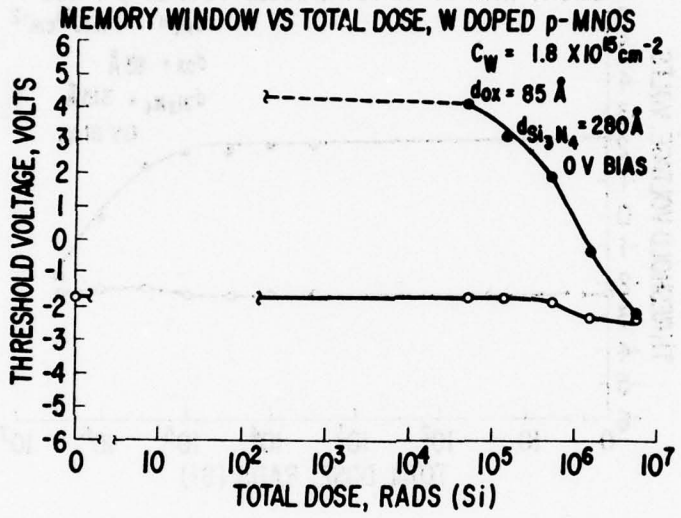


Figure 85. W Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias

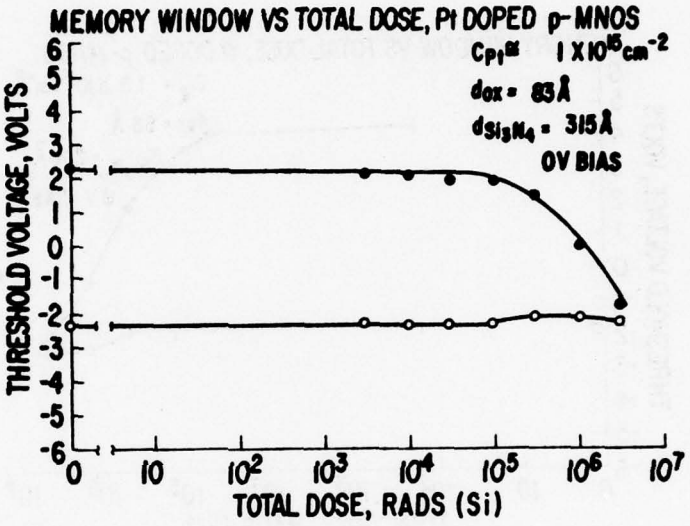


Figure 86. Pt Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias

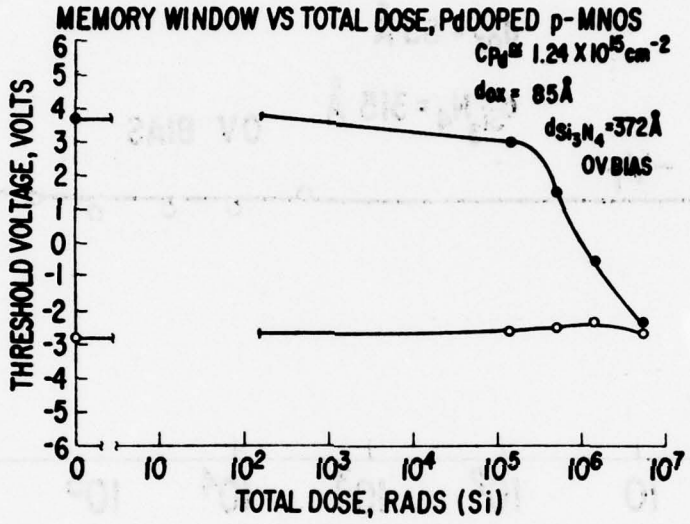


Figure 87. Pd Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias

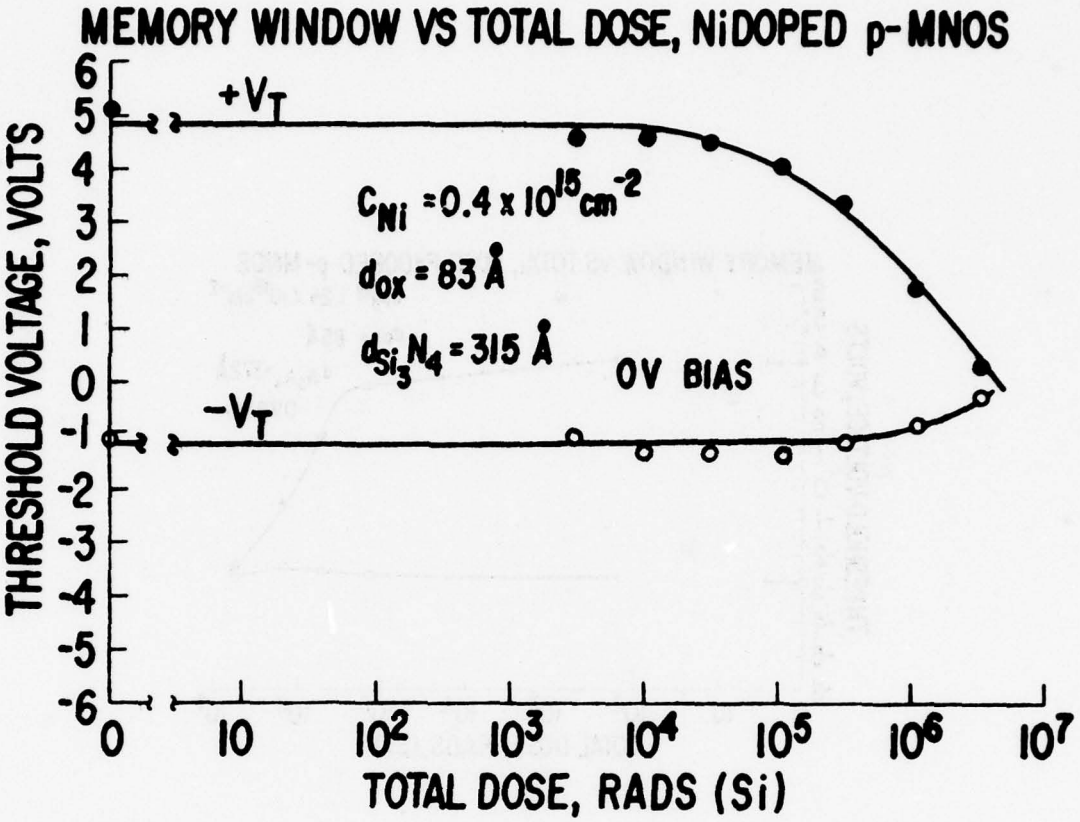


Figure 88. Ni Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias

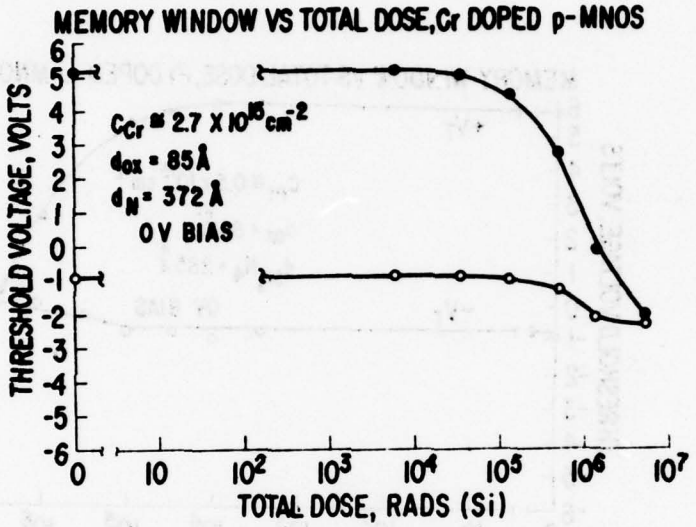


Figure 89. Cr Doped P-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias

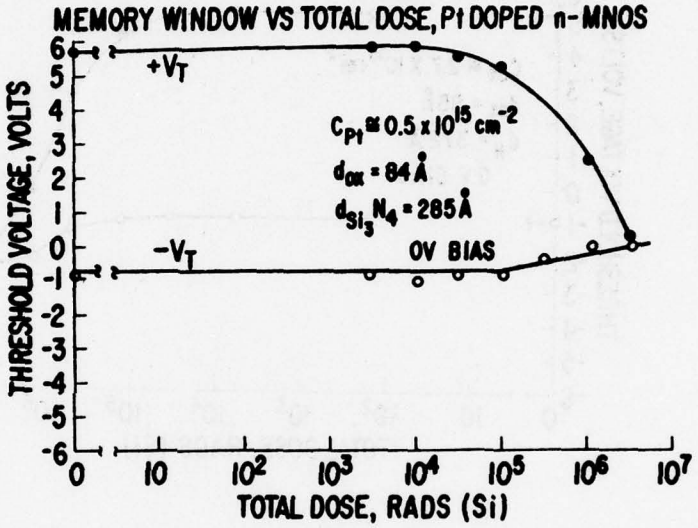


Figure 90. Pt Doped N-Channel Memory Window vs. Total Dose Radiation, Zero Gate Bias

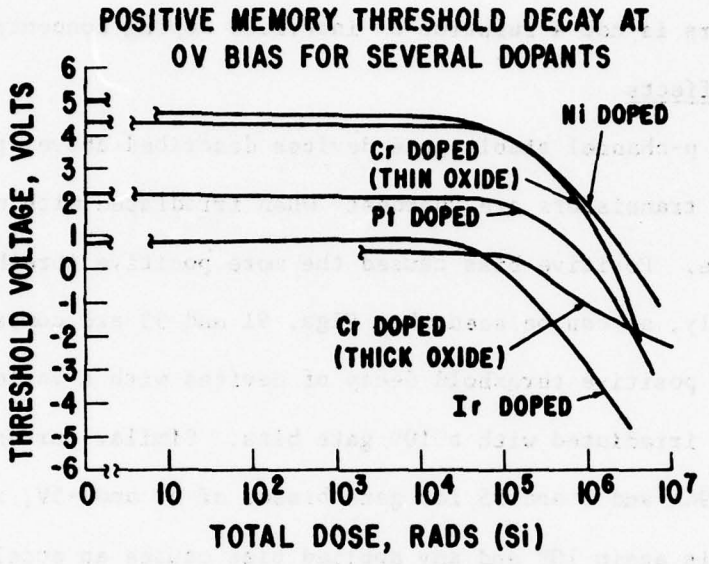


Figure 91. Comparison of Positive Threshold Decay at Zero Bias for Different Dopants During Irradiation

Dopant concentration dependence

Figures 92A and 92B show the memory window vs total dose behavior for two Pt doped memory transistors which differed only in the dopant concentration level. It is seen that the doping level has essentially no effect on total dose hardness. This strongly suggests that the radiation behavior of memory transistors is not a function of interface doping concentration.

Gate bias effects

Just as the p-channel stable gate devices described above, p-channel and n-channel memory transistors are "hardest" when irradiated with no bias applied to the gate. Positive bias caused the more positive thresholds to decay more rapidly, as can be seen when Figs. 91 and 93 are compared. The latter shows the positive threshold decay of devices with a variety of dopants which were irradiated with a 10V gate bias. Similar curves are presented in Figs. 94A and B and 95 for gate biases of 5V and -5V, respectively. Worst case bias is again 10V and any applied bias causes an acceleration of threshold decay.

The effect of gate bias on the radiation response of transistors doped with different metals is shown more clearly in Figs. 96 through 100. Figure 100 highlights the extraordinary sensitivity of platinum doped n-channel positive thresholds to positive bias. While p-channel devices, even under worst case bias, +10V, are stable at least to a total accumulated dose of $3x10^3$ rads (Si), the n-channel devices tested show already a quite large threshold shift at $3x10^3$ rads (Si).

Oxide thickness effects

A limited number of chromium doped thin oxide devices were included in the radiation experiments. The radiation response of typical high and low thresholds among these devices are compared in Fig. 101 with the response of

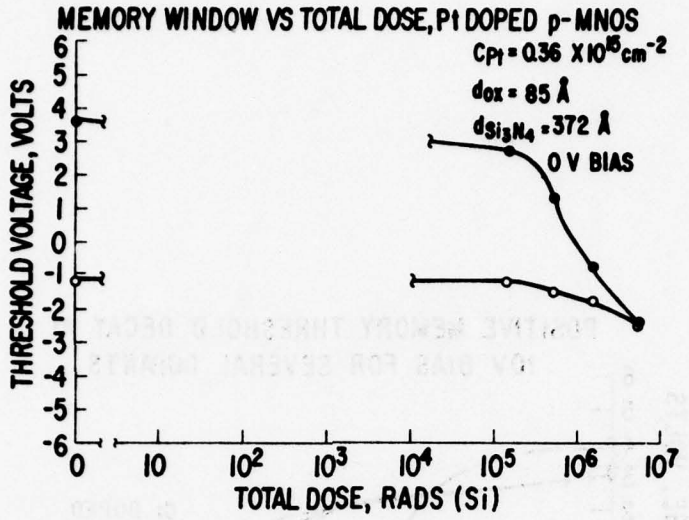


Figure 92A. Memory Window Decay During Irradiation, Low Dopant Concentration

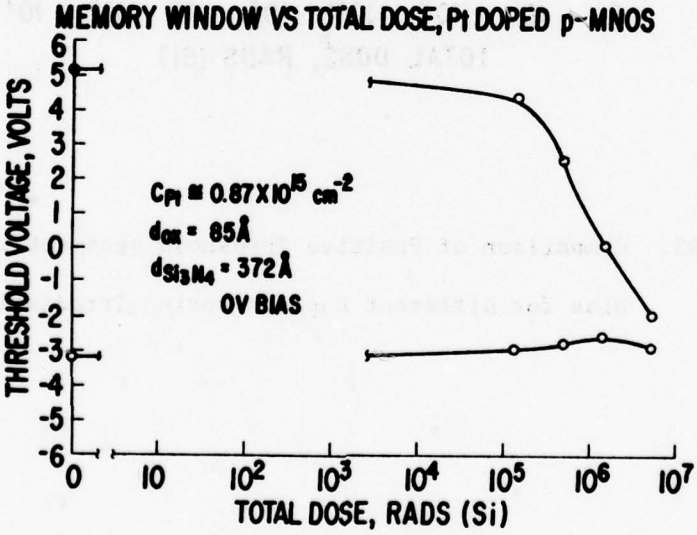


Figure 92B. Memory Window Decay During Irradiation, High Dopant Concentration

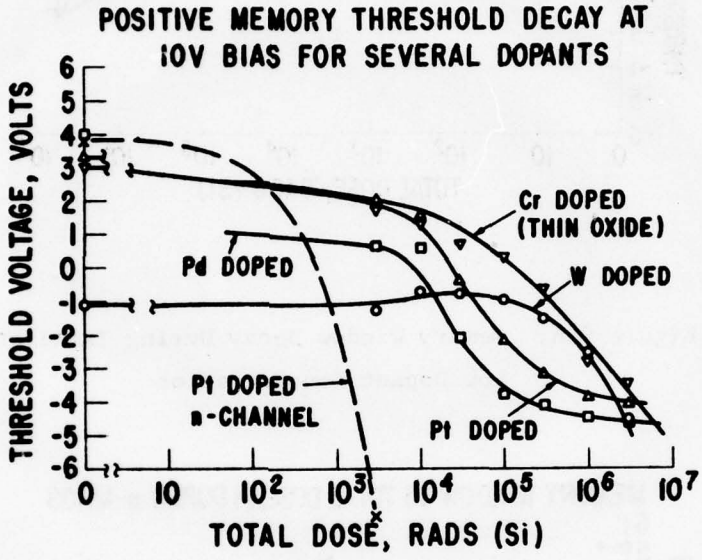


Figure 93. Comparison of Positive Threshold Decay at 10V Bias for Different Dopants During Irradiation

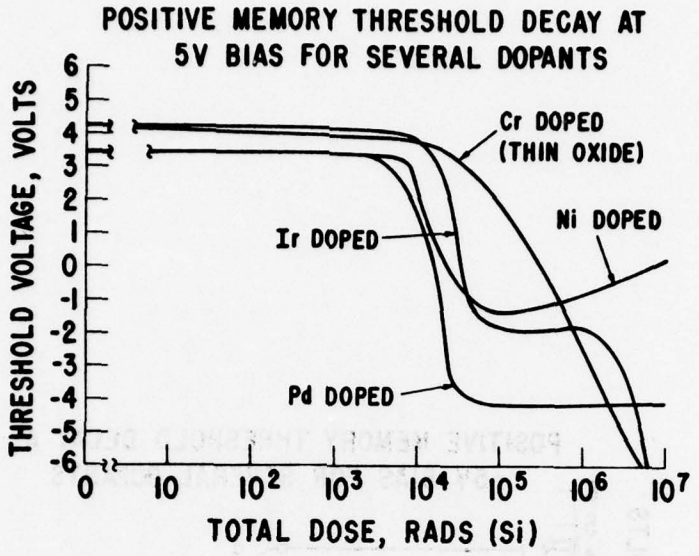


Figure 94A. Comparison of Positive Threshold Decay at 5V Bias for Different Dopants During Irradiation

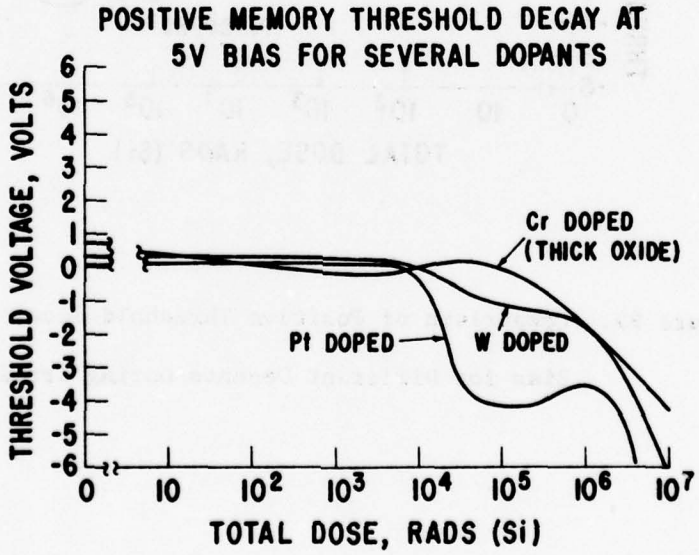


Figure 94B. Comparison of Positive Threshold Decay at 5V Bias for Different Dopants During Irradiation

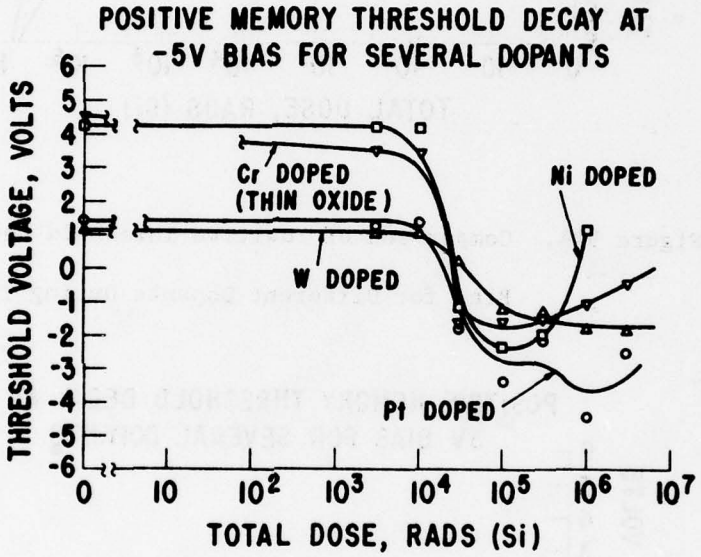


Figure 95. Comparison of Positive Threshold Decay at -5V Bias for Different Dopants During Irradiation

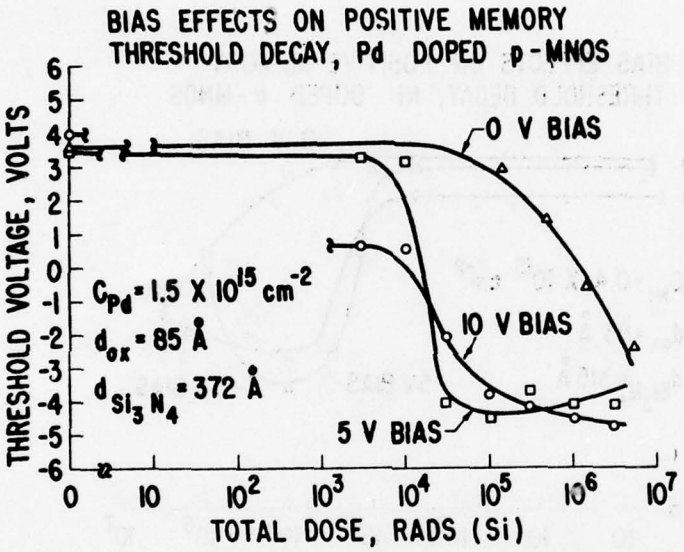


Figure 96. Effects of Different Biases on Pd Doped P-Channel Positive Memory Thresholds

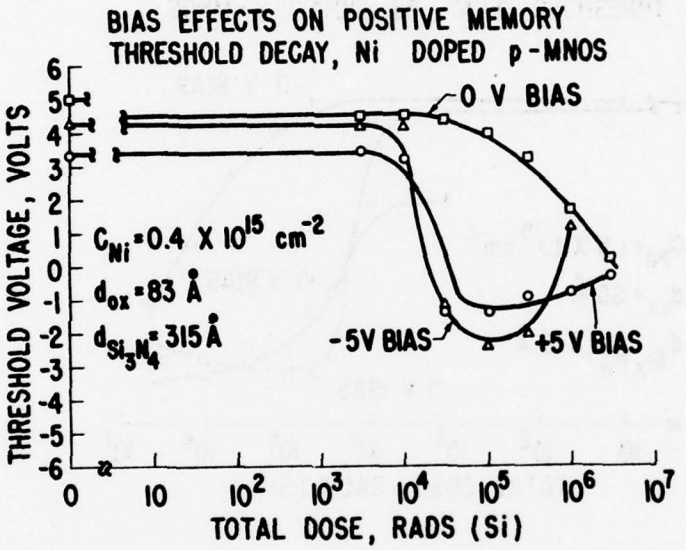


Figure 97. Effects of Different Biases on Cr Doped, P-Channel Positive Memory Thresholds

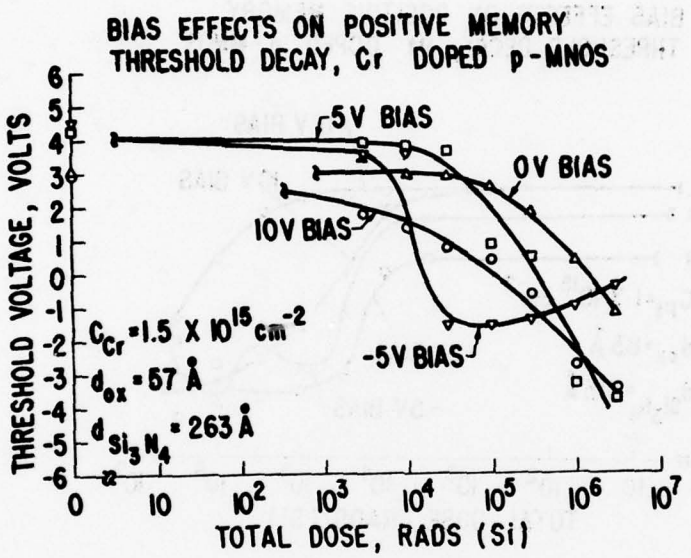


Figure 98. Effects of Different Biases on Cr Doped, P-Channel Positive Memory Thresholds

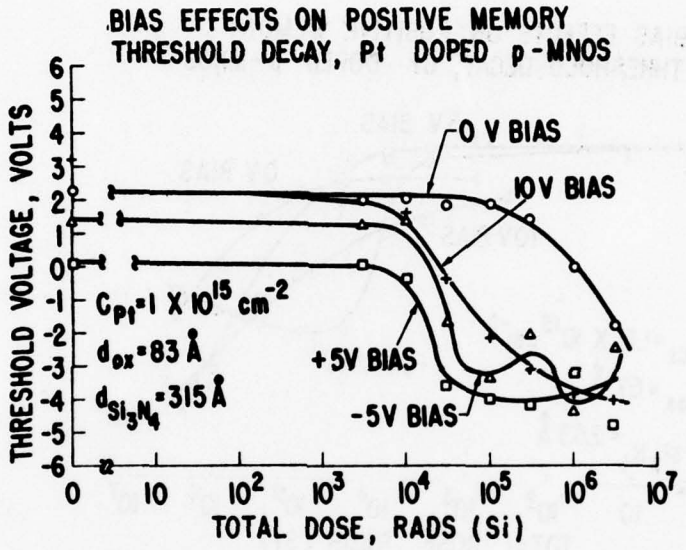


Figure 99. Effects of Different Biases on Pt Doped, P-Channel Positive Memory Thresholds

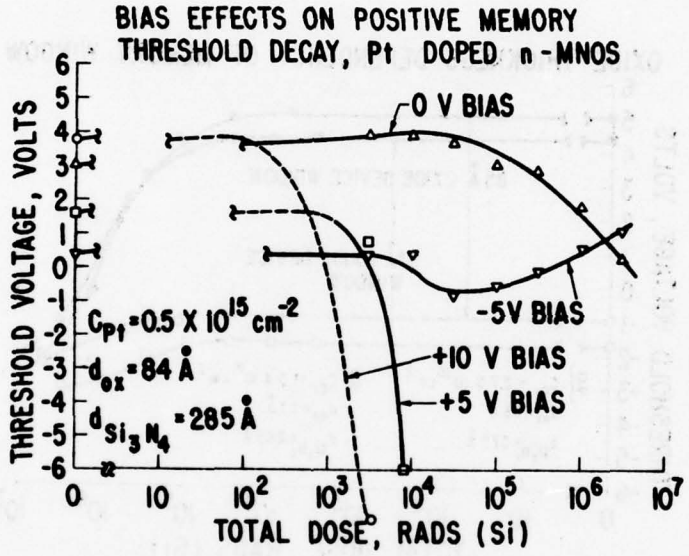


Figure 100. Effects of Different Biases on Pt Doped, N-Channel Positive Memory Thresholds

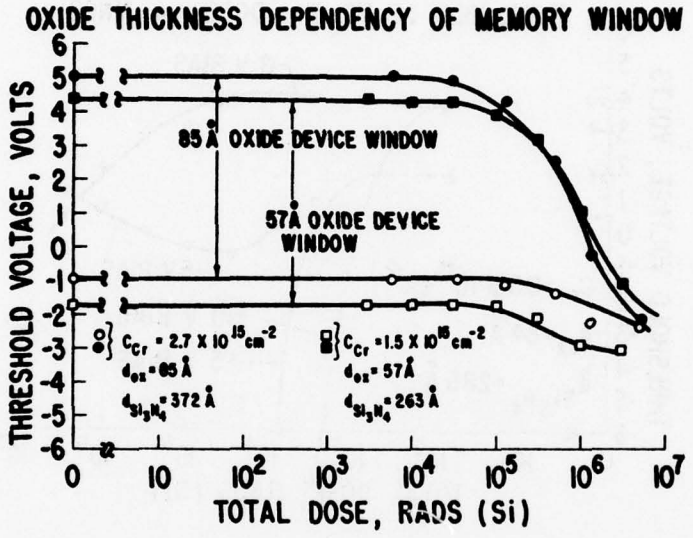


Figure 101. Memory Window Decay During Irradiation for Devices with Different Oxide Thicknesses

thick oxide devices. The two memory windows are virtually identical, even with increasing levels of radiation. This suggests that there is little radiation response dependence on the thickness of the gate oxide over the range of optimum oxide thicknesses.

Ability to rewrite after irradiation

It has been confirmed that for all dopants tested, except tungsten, interface doped devices are fully rewriteable even after a total dose of 3×10^6 rads (Si). Data on tungsten doped devices are inconclusive.

Memory retention after irradiation

After being exposed to a total radiation dose of 3×10^6 rads (Si) with a gate bias of 5V, a platinum doped p-MNOS transistor was rewritten and accelerated retention tests were conducted as described in Section VII. The resultant retention curves are shown in Fig. 102. Retention was 5×10^8 seconds for an initial threshold voltage of 2.8V. This value is in line with pre-radiation figures for devices with similar dopant concentrations, oxide thicknesses, and initial threshold voltages.

CONCLUSIONS

In general, total dose radiation behavior is not greatly different from that of ordinary undoped MNOS devices. For zero or negative gate bias, a hardness level of about 10^5 rads (Si) may be expected, while for positive gate biases it is generally below 10^4 rads (Si). N-channel memory transistors appear to be less radiation hard than p-channel memory transistors under positive gate bias. On the other hand, for stable gate devices, Cr doping appears to increase total dose hardness by about one order of magnitude. In all cases, the threshold voltage becomes more negative with increasing dose. The threshold voltage decay with radiation is always faster for the more positive threshold state than the more negative state.

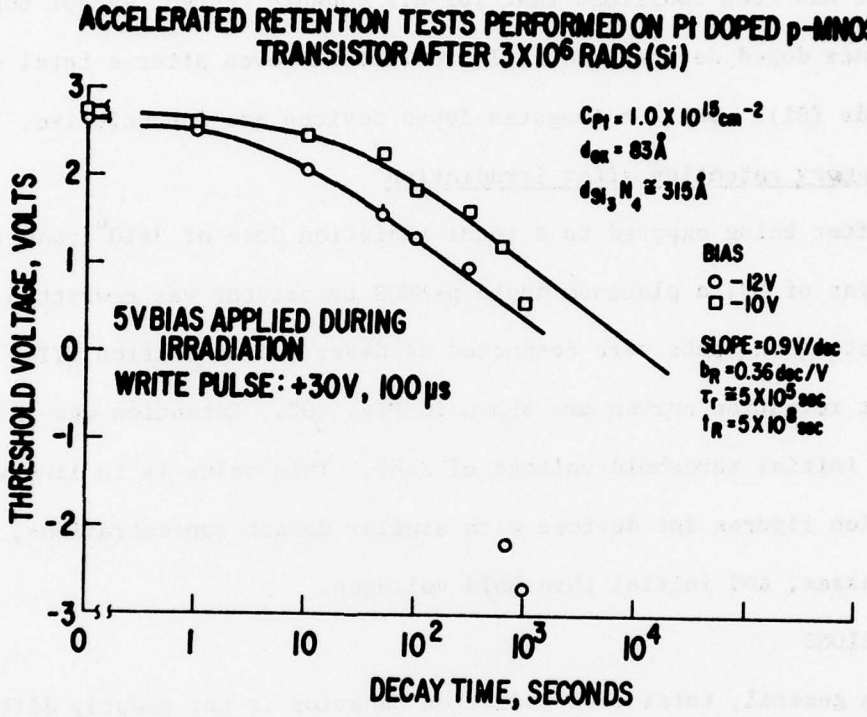


Figure 102. Accelerated Retention Tests Performed on Pt Doped, P-Channel Transistors After a Total Dose of 3×10^6 Rads (Si)

SECTION XI

PROCESS YIELD ASSESSMENT

P-CHANNEL YIELD

During the first phase of the MNOS contract period, only aluminum gate p-channel varactors and transistors were fabricated. All effort was directed toward optimizing the processing sequence, particularly the interface doping step, so as to produce acceptable devices. At the end of that phase, certain dopants, dopant concentrations and gate oxide thicknesses were identified as "optimum". The p-channel process could then be implemented to produce optimum memory devices with a very high yield. Wafers processed to give memory varactors only exhibited yields of 90% or more. When discrete p-channel memory transistors were fabricated, a similar high yield was achieved over the range of optimum parameters. However, the yield dropped to zero when attempts were made to fabricate both stable gate and memory transistors (as opposed to memory varactors) on the same wafer. Acceptable stable gate transistors and memory varactors were fabricated on the same wafer but memory transistors on the same wafer, while behaving like stable gate transistors, could not be written. This was in spite of the fact that memory varactors could simultaneously be made on the same wafer and exhibited memory characteristics. The reason is not understood, but must be related to step 7 in the process.

N-CHANNEL YIELD

Since the interface doped memory device tends to store "excess" electrons rather than holes, the memory window is predominantly positive. Consequently, the n-channel device, which has the memory window in the non-conducting (positive) gate potential region, is more desirable from circuit considerations.

considerations.

A new fabrication sequence was designed by which n-channel polysilicon gate stable gate transistors and aluminum gate memory transistors could be processed on the same wafer. While experiments were conducted on polysilicon gate fabrication techniques, n-channel memory varactor wafers were processed. Using these wafers, n-channel memory characteristics like write speed, retention, saturation window and endurance were examined and found to be, in all essential respects, very similar to those of p-channel memory varactors. These wafers also exhibited very high yield percentages (on the order of 80%) for "optimum" fabrication parameters. This is illustrated in Figs. 103, 104, and 105, in which yields are shown for various dopants, dopant concentrations, and oxide thicknesses, for n-channel memory varactors.

Discrete, n-channel memory transistors were next fabricated and their yields were measured. To check for parameter spreads within a particular wafer, Pt-doped and Cr-doped n-channel wafers were examined. The parameters measured in this test were the original (before any writing) threshold voltage, the threshold voltage after writing with a +25V, 100 μs pulse, and the threshold voltage after writing with a -25V, 100 μs pulse. This test was applied to the same transistor in every chip location in each wafer. The source-drain voltage was 5V, and the threshold voltage was taken as the gate voltage to give a 1 ma current. These test results are shown in the form of wafer maps in Figs. 106 and 107 for Cr and Pt doped MNOS wafers, respectively.

The doping concentration varied in a wedge profile across the wafer between the values of .007 to 1.9×10^{15} cm^{-2} for Cr and .03 and 0.8×10^{15} cm^{-2} for Pt. There was little discernable dependence of the test data on doping concentration in the range used, as was anticipated from previous experience with p-channel transistors and n-channel varactors. However, the boundary

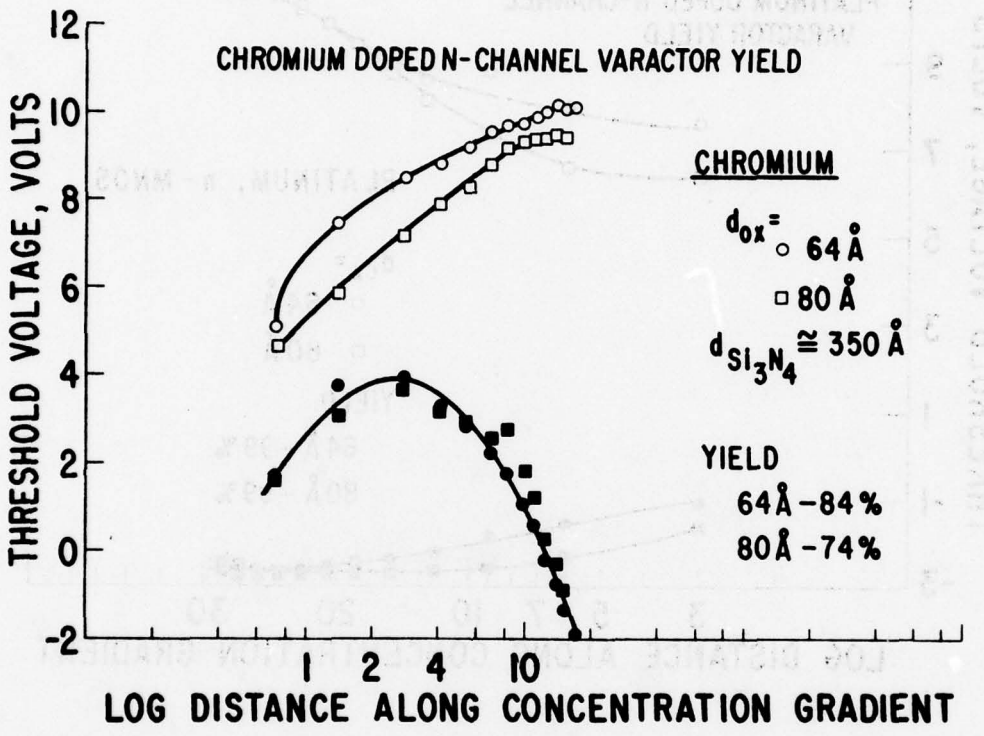


Figure 103. Chromium Doped N-Channel Varactor Yield

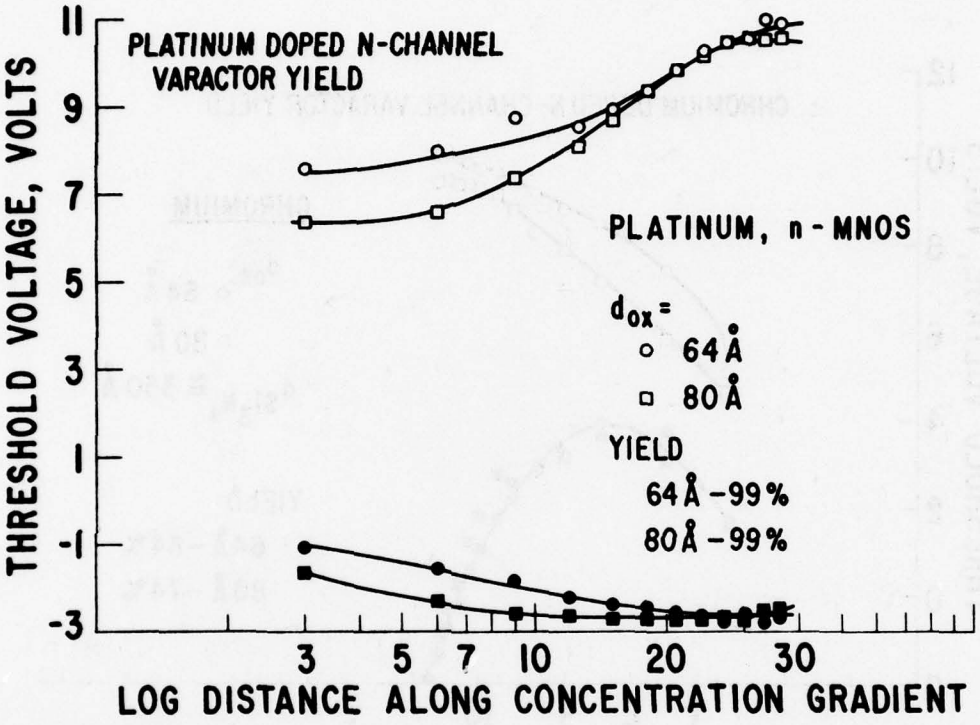


Figure 104. Platinum Doped N-Channel Varactor Yield

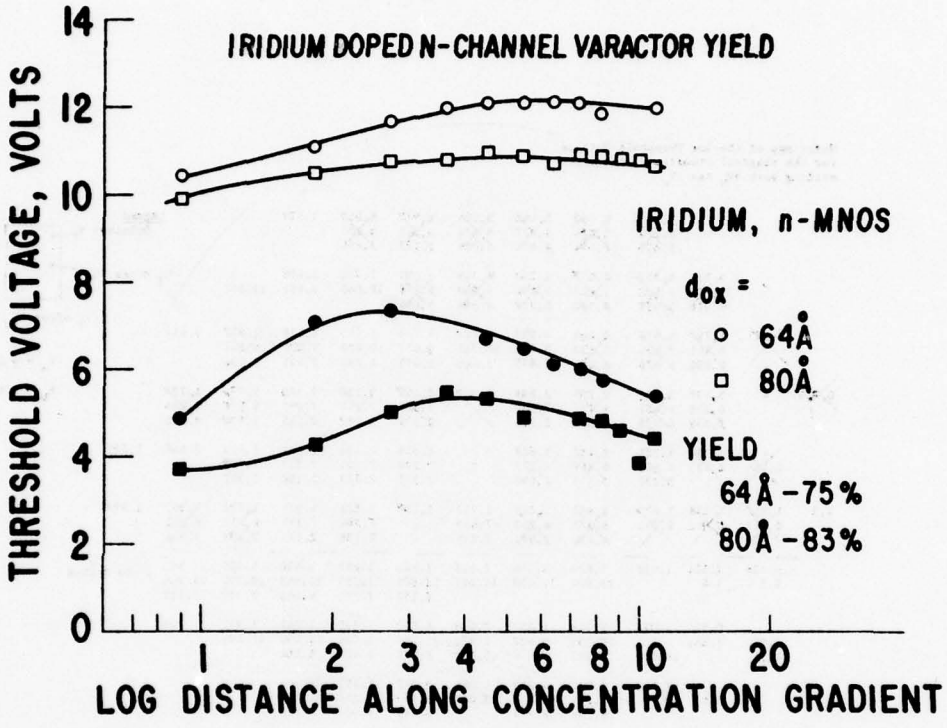


Figure 105. Iridium Doped N-Channel Varactor Yield

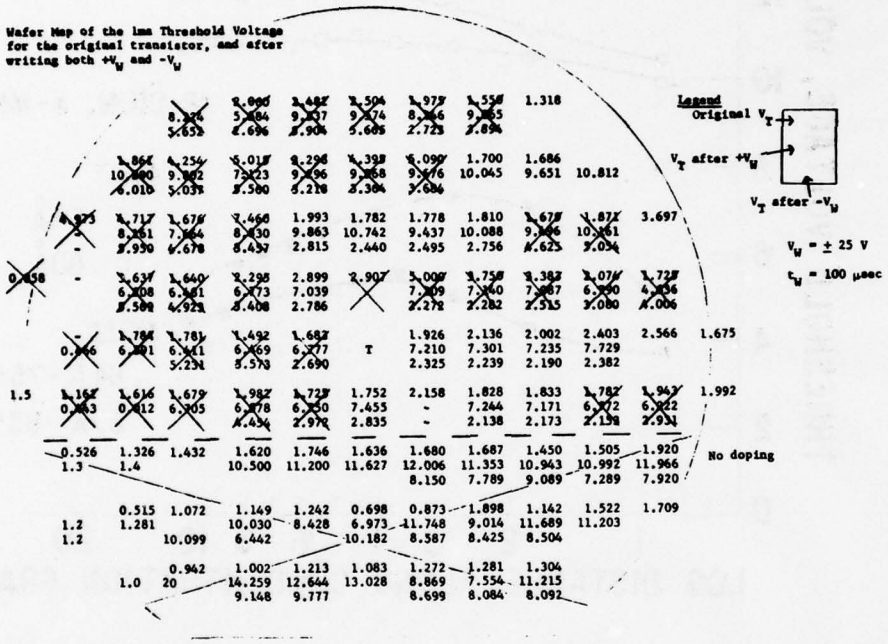


Figure 106. Yield Survey Map of Chromium Doped N-Channel Memory Transistors

AD-A068 493 GENERAL ELECTRIC CORPORATE RESEARCH AND DEVELOPMENT --ETC F/G 9/1
INTERFACE DOPING OF MNOS TRANSISTORS.(U)
JUN 78 C A NEUGEBAUER, M M BARNICLE F33615-76-C-1035

UNCLASSIFIED SRD-78-097 AFAL-TR-78-87 NL

3 OF 3
AD A068493

END
DATE FILMED
6 -79
DDC

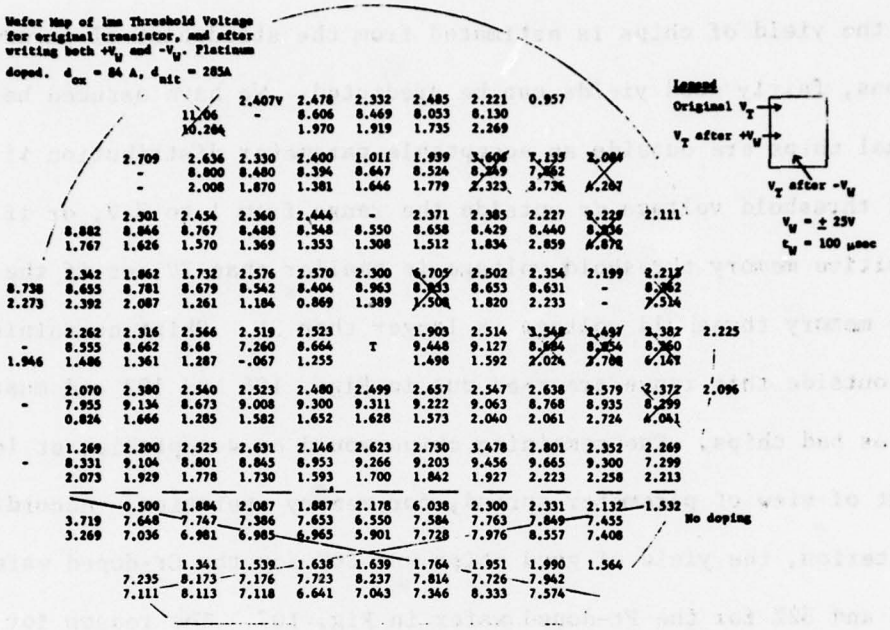


Figure 107. Yield Survey Map of Platinum Doped N-Channel Memory Transistors

between dopant and no-dopant regions was very clearly visible, since the $-V_w$ pulse would not write in undoped devices. This is responsible for the small memory window in the section below the dotted line in Figs. 106 and 107.

If the yield of chips is estimated from the standpoint of parameter distributions, fairly good yields can be predicted. We have assumed here that individual chips are outside an acceptable parameter distribution if the original threshold voltage is outside the range from 1 to 3 V, or if the more positive memory threshold voltage is smaller than 7V, or if the more negative memory threshold voltage is larger than 3V. Chips containing transistors outside this range are x-ed out in Figs. 106 and 107 and must be counted as bad chips. The remaining chips would be acceptable, at least from the point of view of parameter spread, for memory operation. According to this criterion, the yield of good chips was 26% for the Cr-doped wafer in Fig. 106 and 82% for the Pt-doped wafer in Fig. 107. The reason for rejection in most cases was too small a memory window. For each wafer, oxide and nitride thicknesses were 84Å and 285Å, respectively.

Next, wafers were fabricated with only polysilicon stable gate transistors. The procedure is covered in Section III under "Fabrication of N-Channel Devices". Stable gate oxides are 1000Å and the polysilicon thicknesses is 8000Å. The results of a yield survey performed on a four-wafer run in which poly gate transistors only were fabricated are listed below. One transistor from over 10% of the chips on each wafer was measured. Each transistor had to meet the minimum criteria that its threshold voltage fall between zero and 2V and a leakage current of less than 5 μA. Shorts through through the gate oxide were not a common reason for rejection. More frequently, lack of contact with the gate, due to incomplete etching, was the

suspected cause of rejection. Yields are shown in Table 14.

Table 14

RESULTS OF YIELD SURVEY OF POLYSILICON STABLE GATE N-CHANNEL TRANSISTOR WAFERS

Wafer	Yield
AE-28-4A	44%
-4B	96%
-4C	23%
-4D	80%

Thus the results of yield surveys on wafer runs in which memory transistors only or polysilicon stable gate transistors only were fabricated, were highly encouraging. It remained to produce both types of transistors on the same wafer. The total process would require close to 80 distinguishable steps - many more than would be required to produce each type of transistor alone. Seven wafer runs (a total of 28 wafers) were produced in an effort to make stable gate and memory transistors on the same wafers. In no instance, however, was it possible to produce memory transistors which exhibited memory characteristics when processed on the same wafer with polysilicon stable gate transistors. The memory transistors did display good characteristic curves with positive threshold voltages, but no memory window could be written, i.e., they behaved like stable gate transistors. Paradoxically, memory varactors fabricated on the same wafers exhibited normal memory behavior and were completely writable.

Table 15 contains pertinent process parameters for a run of wafers containing both stable gate and memory transistors as well as memory varactors. Table 16 contains the results of a yield survey for this run. Some of the memory transistors are partially or fully protected by a 500Å protective

TABLE 15

IMPORTANT PROCESS PARAMETERS FOR WAFER RUN #9

Wafer	d_{ox}	$d_{Si_3N_4}$	Dopant	Concentration Range
AE28-9A	~ 80Å	~ 300Å	Pd	0 to 3.3×10^{15} cm^{-2}
-9B	"	"	Pt	0 to 2.4×10^{15}
-9C	"	"	Pt	0 to 2.4×10^{15}
-9D	"	"	Pd	0 to 3.3×10^{15}

TABLE 16

DEVICE YIELDS FOR WAFER RUN #9

Wafer	Device	Yield, %
9A	stable Si gate	6
	fully protected Al-gate (stable gate)	79
	partially protected Al-gate (stable gate)	87
	varactors	0
	memory transistors	0
9B	stable Si-gate	87
	fully protected Al-gate	80
	partially protected Al-gate	84
	varactors	87
	memory transistors	0
9C	stable Si-gate	67
	fully protected Al-gate	56
	partially protected Al-gate	59
	varactors	65
	memory transistors	0

TABLE 16 (Cont'd.)

Wafer	Device	Yield, %
9D	stable Si-gate	88
	fully protected Al-gate	99
	partially protected Al-gate	94
	varactors	0

oxide. While these transistors do not display memory characteristics, their threshold voltages, V_T, leakage currents, I_L, and the slope of the drain current vs. gate voltage curves were (related to g_m) measured. The following criteria were used to determine the "chip yield" in each wafer:

- Memory window @ $\pm$ 30V, 1 ms: $W \geq 4V$
- Polysilicon gate transistor: $0 \leq V_T \leq 2V$

  $I_L \leq 5\ \mu A$

  Al-gate memory transistors: $0 \leq V_T$ (original) $\leq 4V$

  $I_L \leq 5\ \mu A$

  (no memory characteristics)

Figure 108A contains the information obtained from stable gate devices on wafer -9A. Each small box represents one chip location on the wafer. The topmost number is the threshold voltage. The second number is the slope of the I_D vs. V_G curve, given in A/V which is proportional to the gain. The last number is the device leakage current at $V_G = 0$, $V_D = 10V$. Figure 108B gives the same information for fully protected memory devices and Fig. 108C for the partially protected transistors. The varactor memory windows are presented in Fig. 108D. The same data for the other three wafers are similarly given in Figs. 109A through D, 110A through D, and 111A through D, respectively.

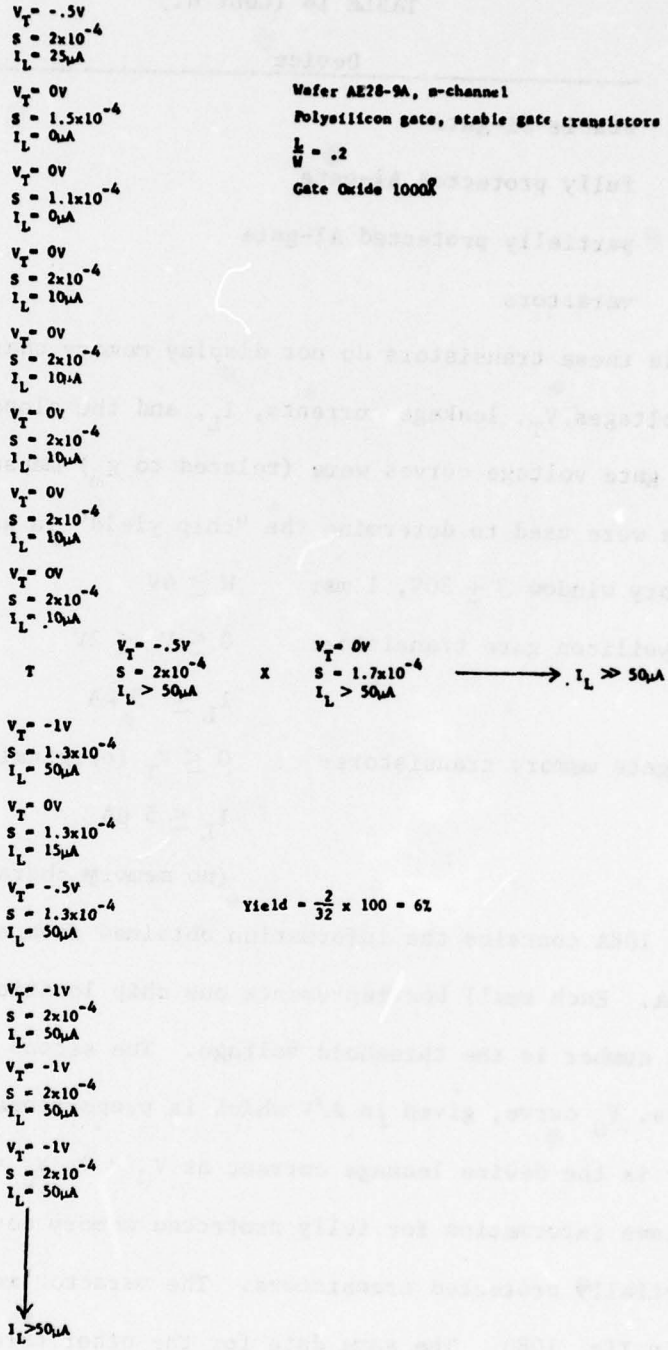


Figure 108A. Yield Survey of Device Characteristics on Wafer A28-9A, Stable Gate and Memory Devices

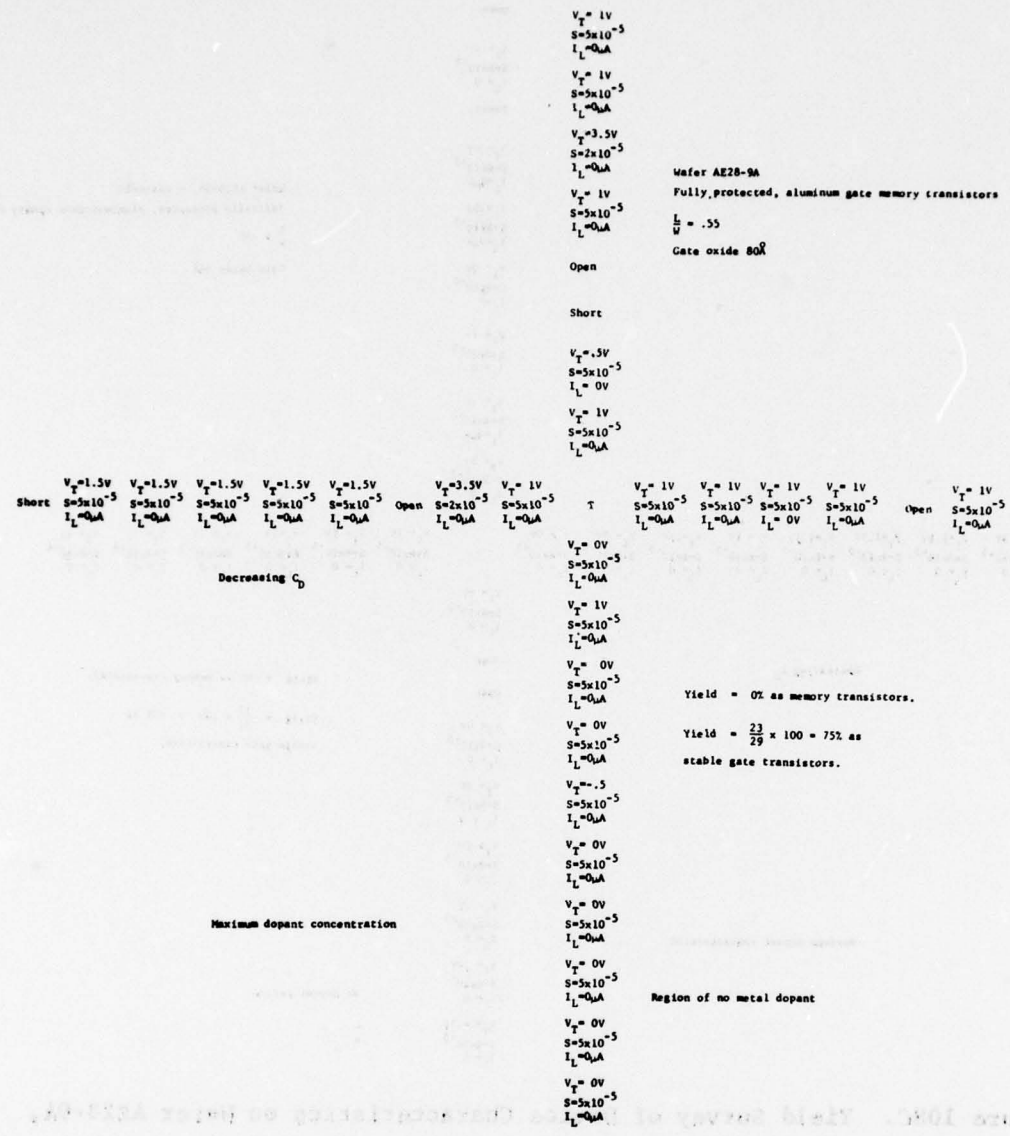


Figure 108B. Yield Survey of Device Characteristics on Wafer AE28-9A, Stable Gate and Memory Devices

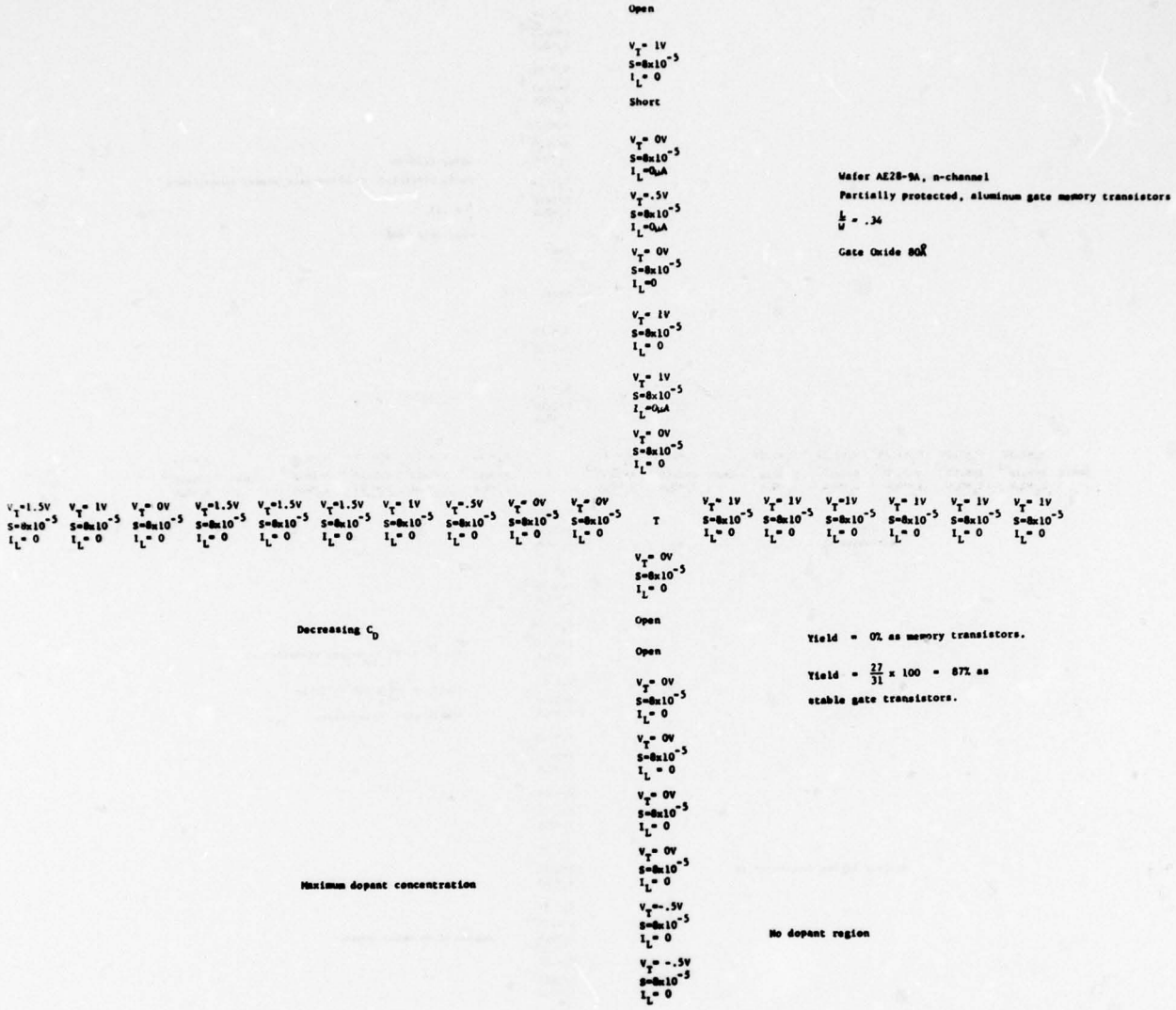


Figure 108C. Yield Survey of Device Characteristics on Wafer AE28-9A, Stable Gate and Memory Devices

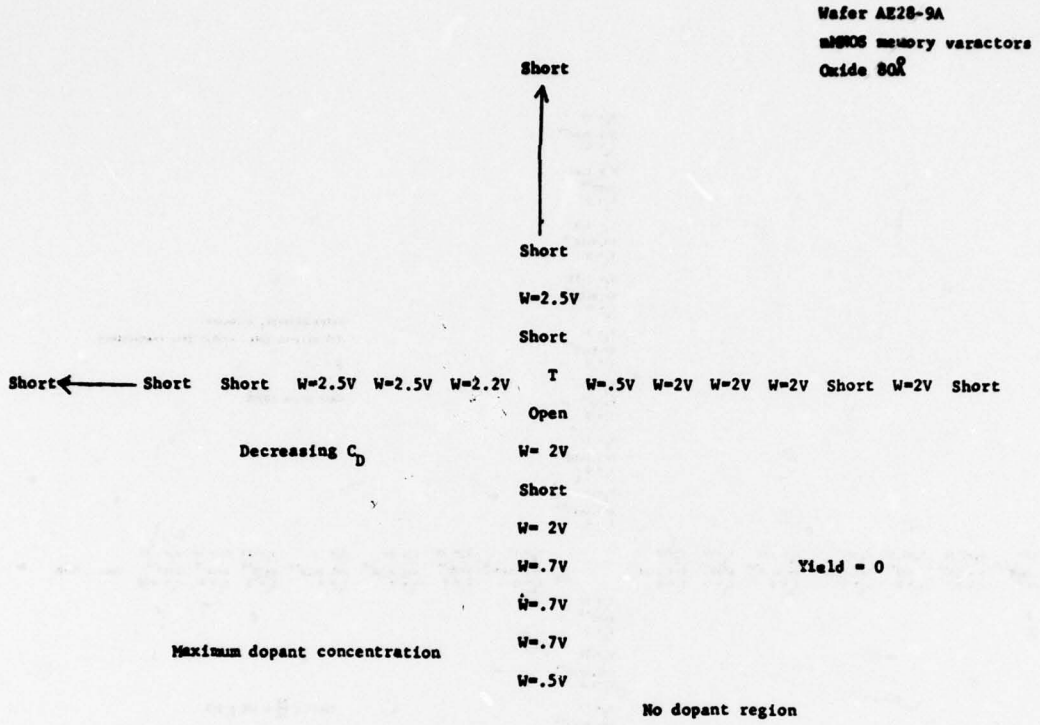


Figure 108D. Yield Survey of Device Characteristics on Wafer AE28-9A, Stable Gate and Memory Devices

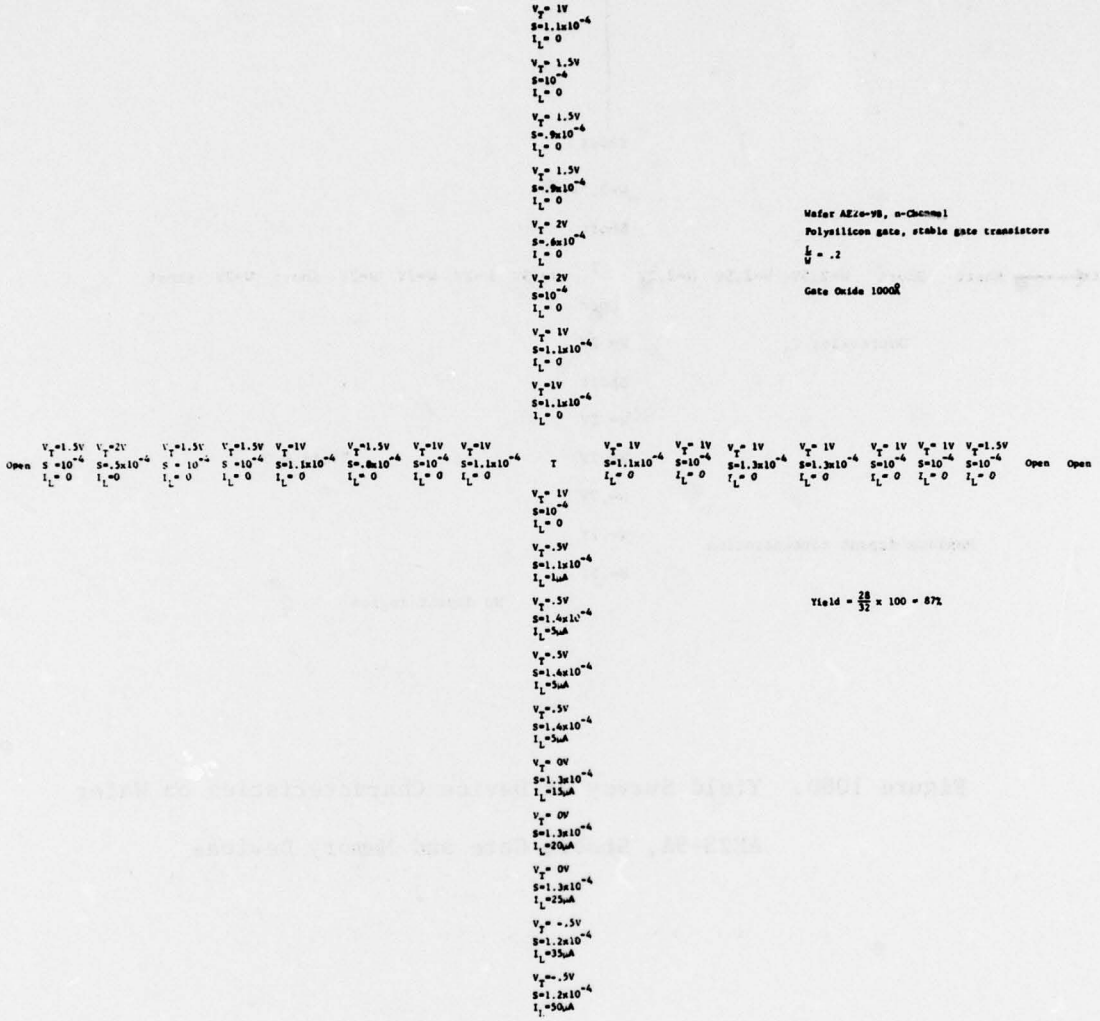


Figure 109A. Yield Survey of Device Characteristics on Wafer A28-9B, Stable Gate and Memory Devices

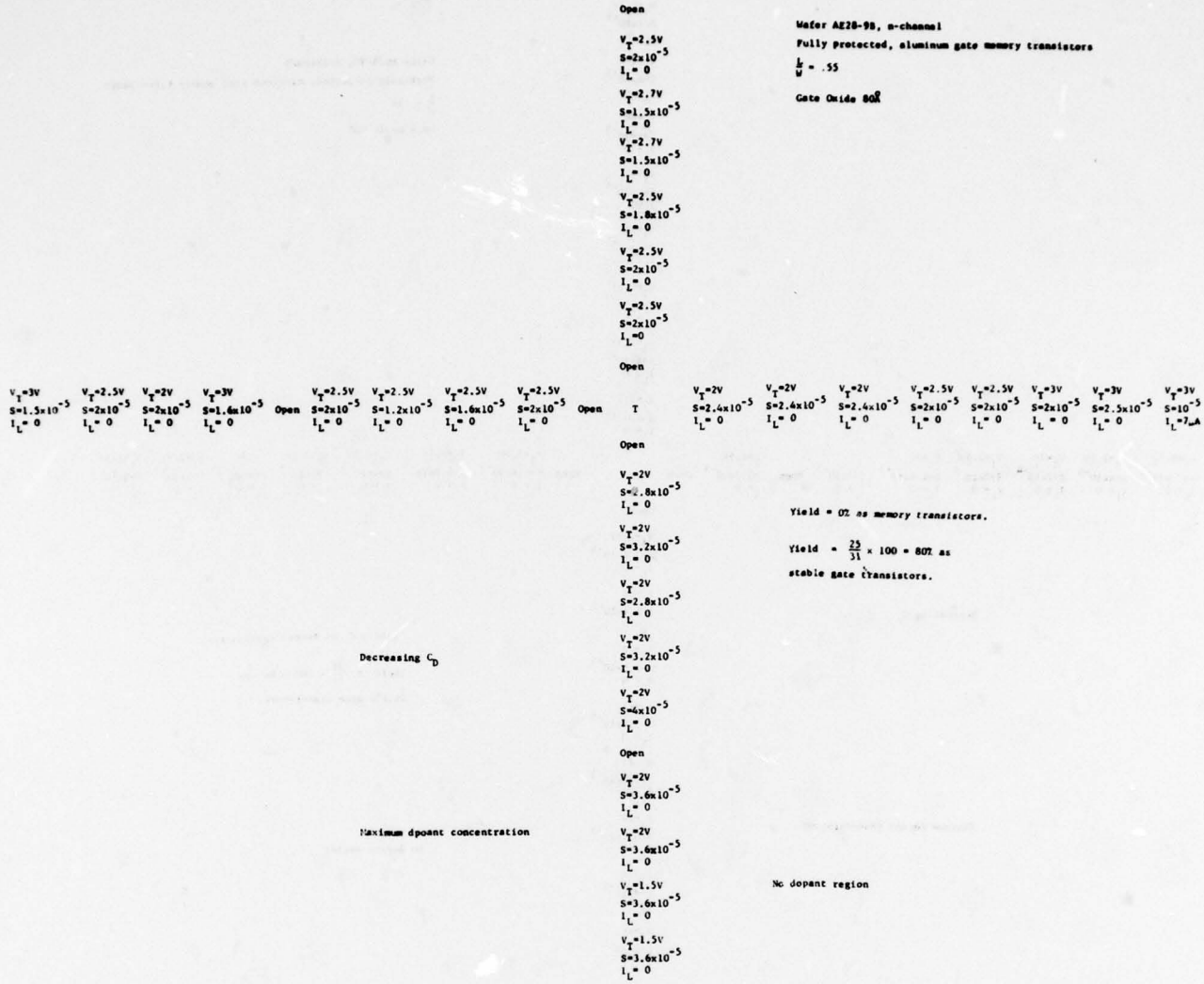


Figure 109B. Yield Survey of Device Characteristics on Wafer A28-9B, Stable Gate and Memory Devices

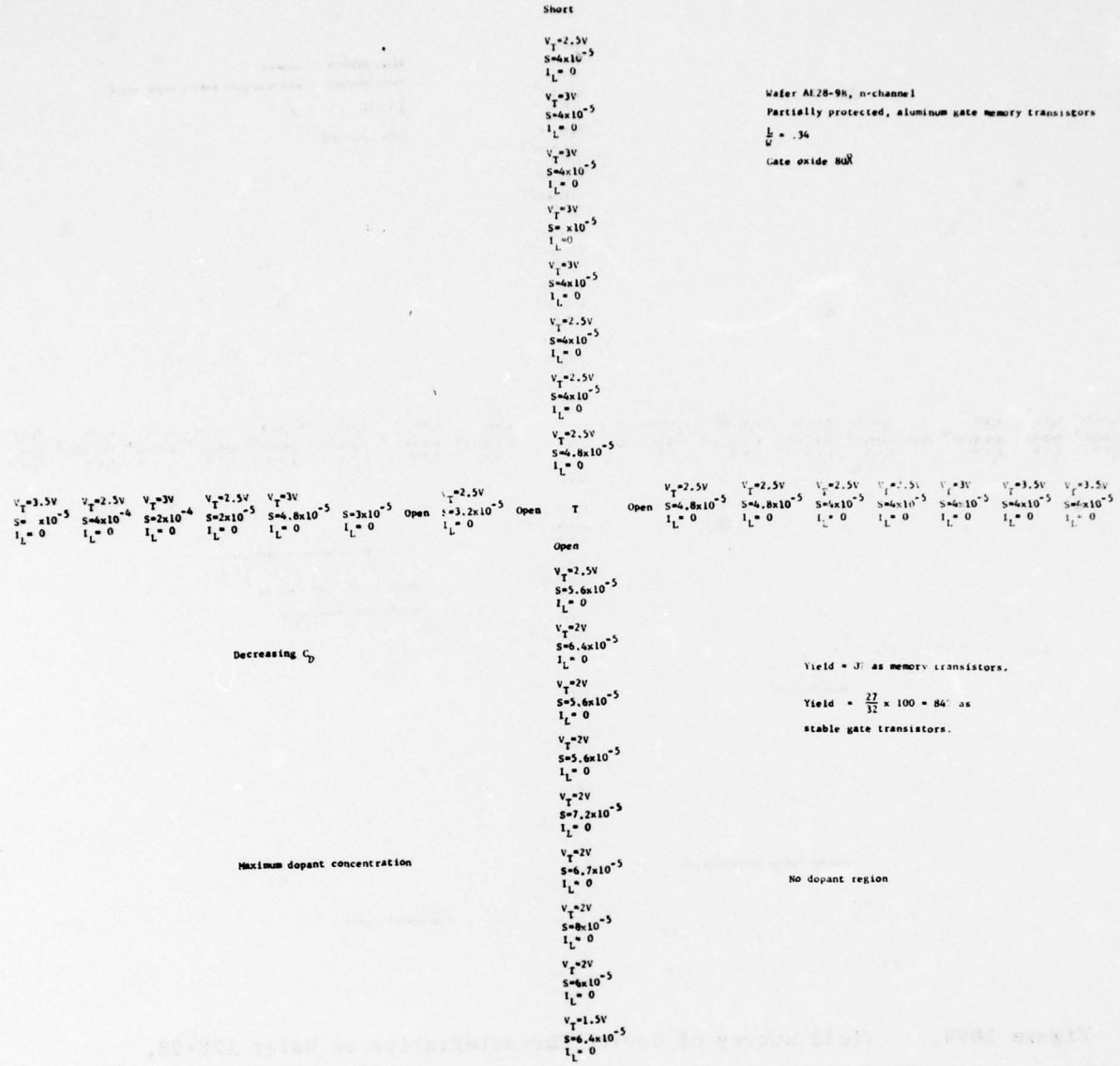


Figure 109C. Yield Survey of Device Characteristics on Wafer A28-9B, Stable Gate and Memory Devices

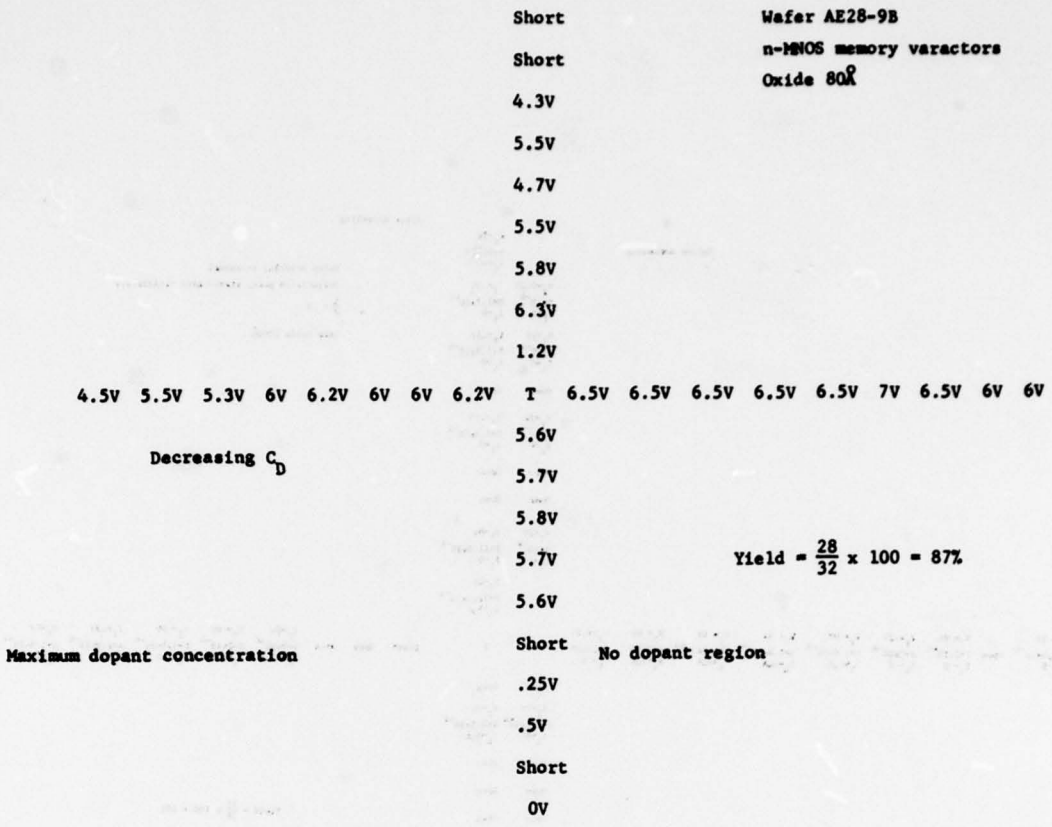


Figure 109D. Yield Survey of Device Characteristics on Wafer A28-9B, Stable Gate and Memory Devices

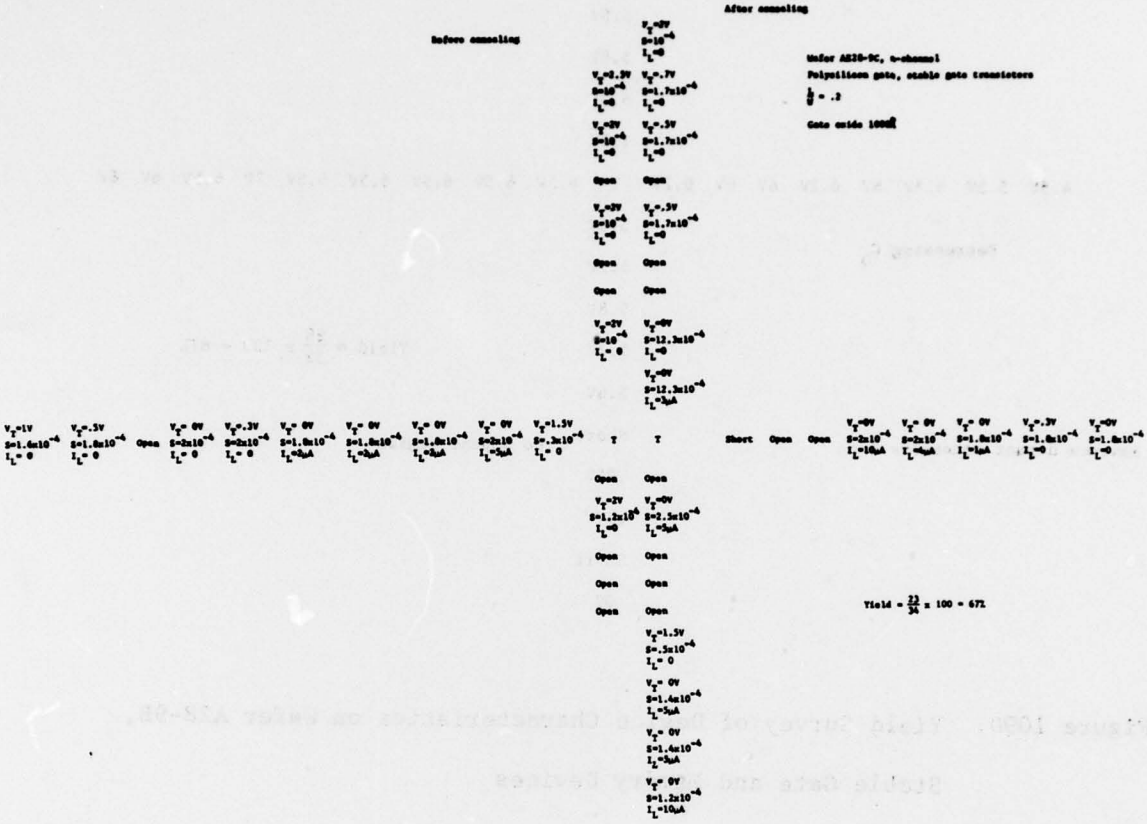


Figure 110A. Yield Survey of Device Characteristics on Wafer A28-9C, Stable Gate and Memory Devices

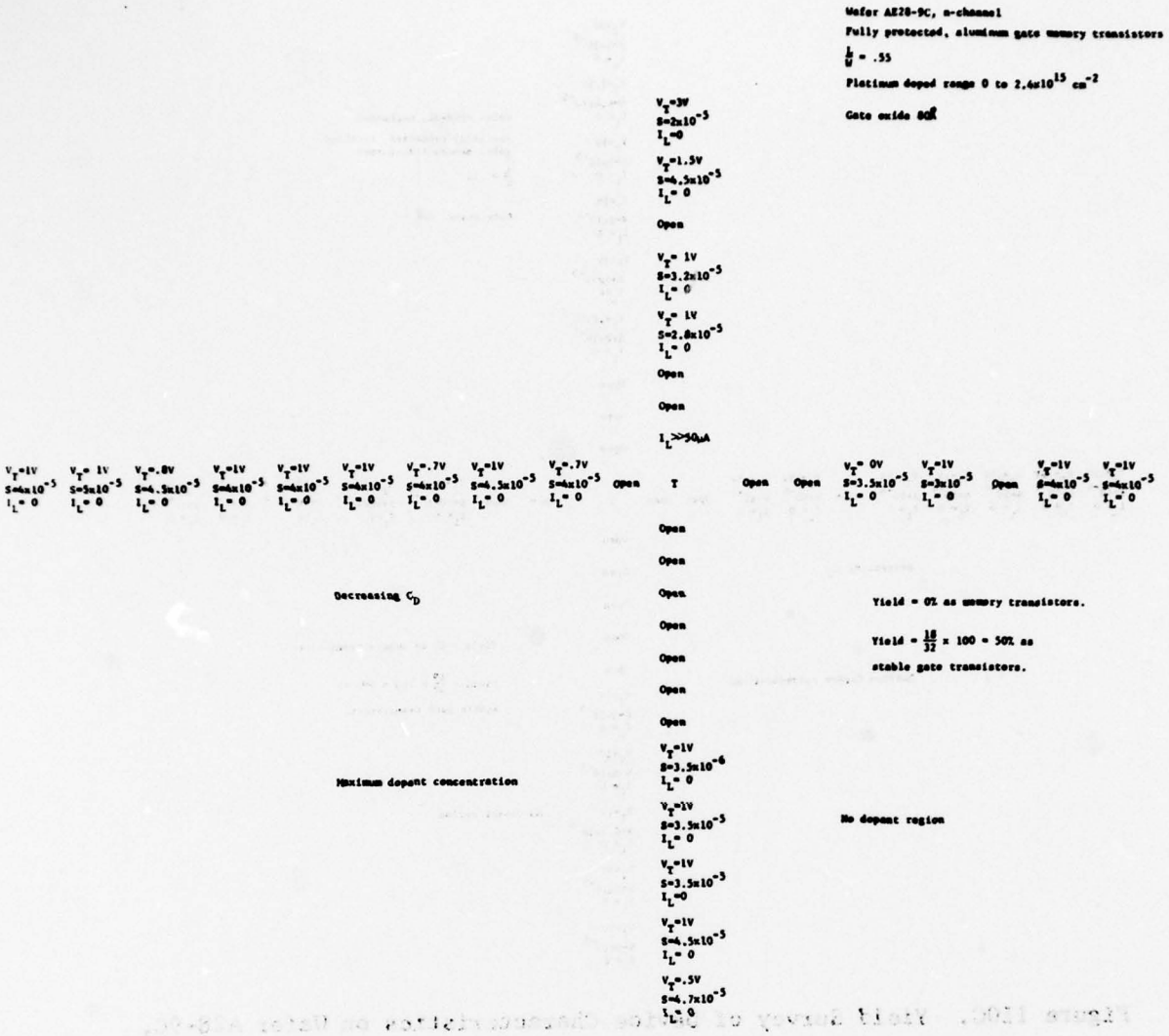


Figure 110B. Yield Survey of Device Characteristics on Wafer A28-9C, Stable Gate and Memory Devices

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

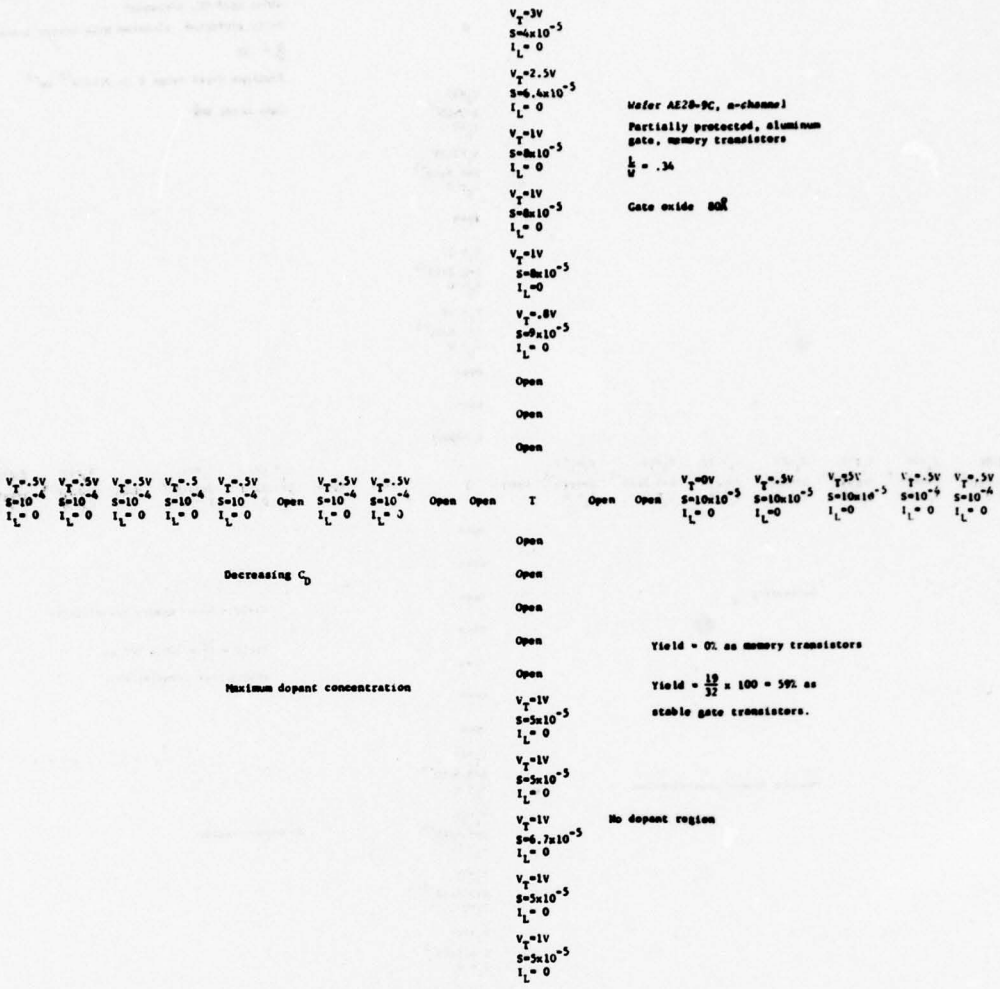


Figure 110C. Yield Survey of Device Characteristics on Wafer A28-9C, Stable Gate and Memory Devices

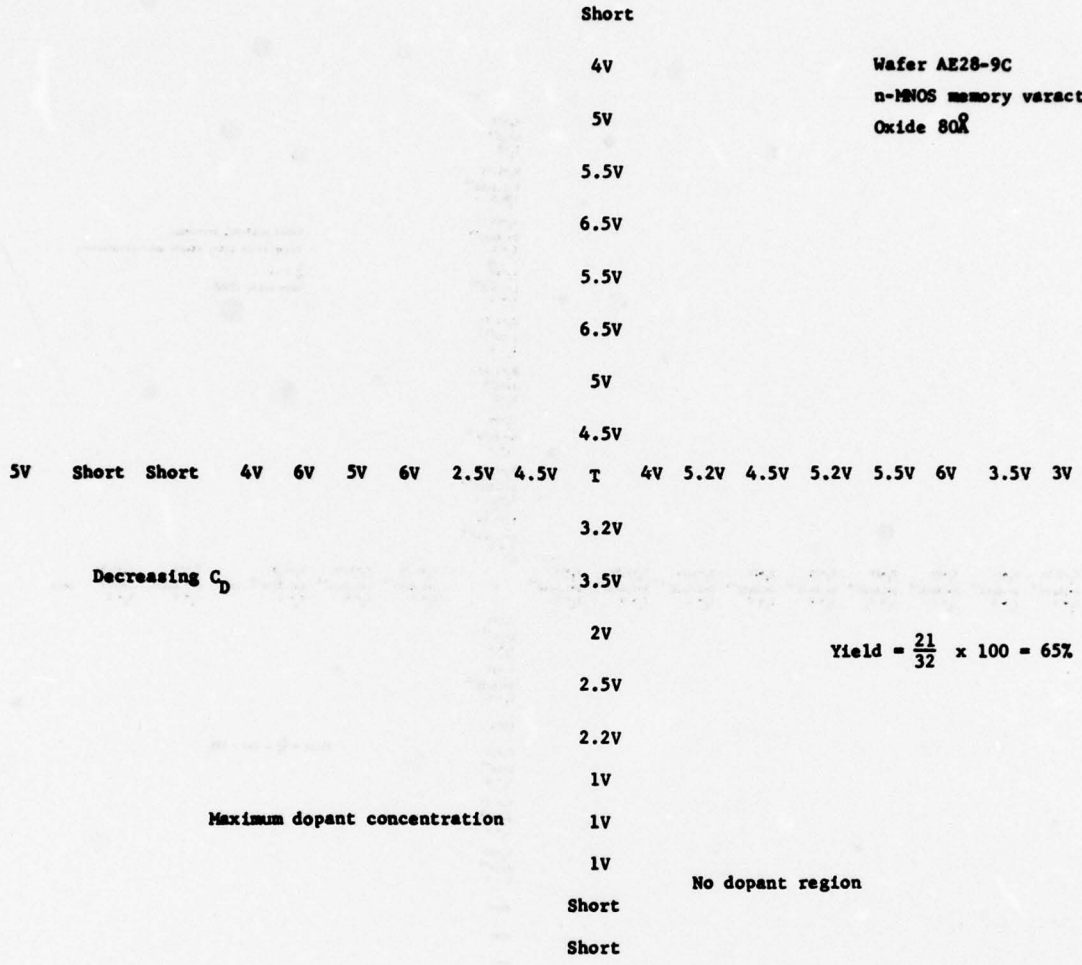
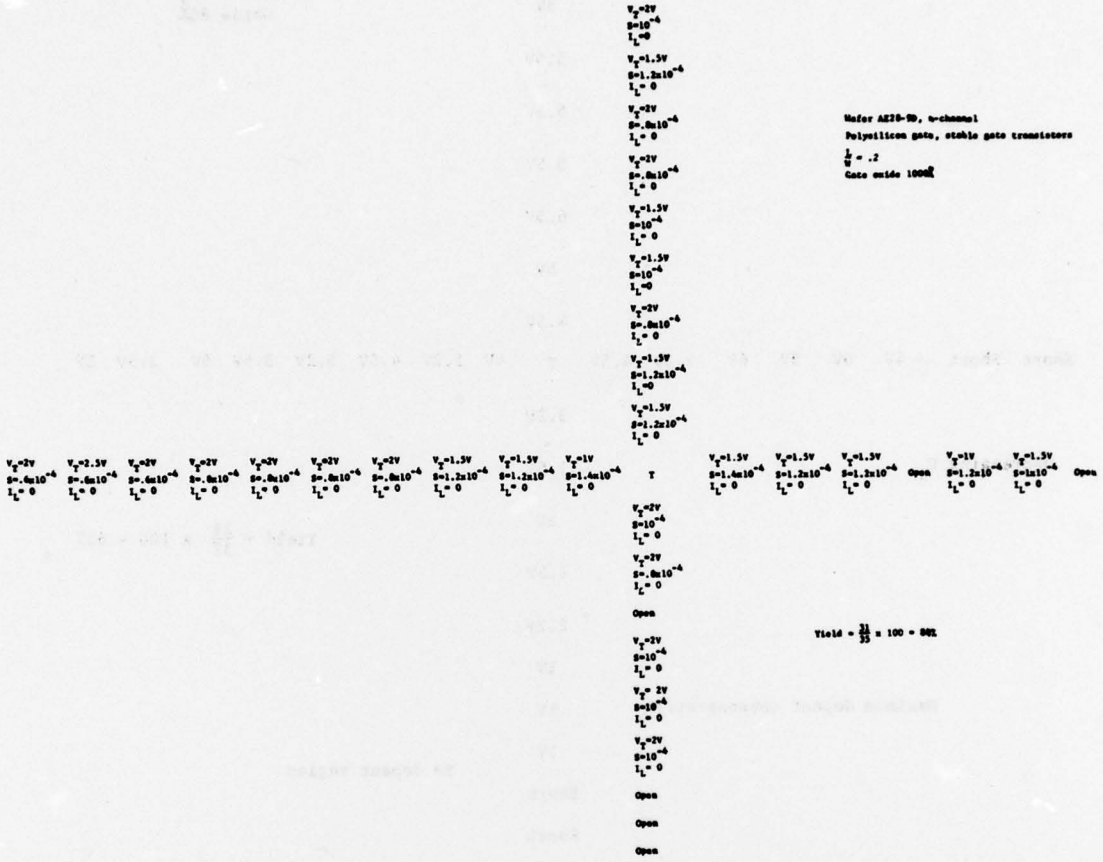


Figure 110D. Yield Survey of Device Characteristics on Wafer A28-9C, Stable Gate and Memory Devices


Wafer A28-9D, n-channel
Polysilicon gate, stable gate transistors
$\frac{L}{W}$ = .2
Gate oxide 1000Å
Open
Open
Open

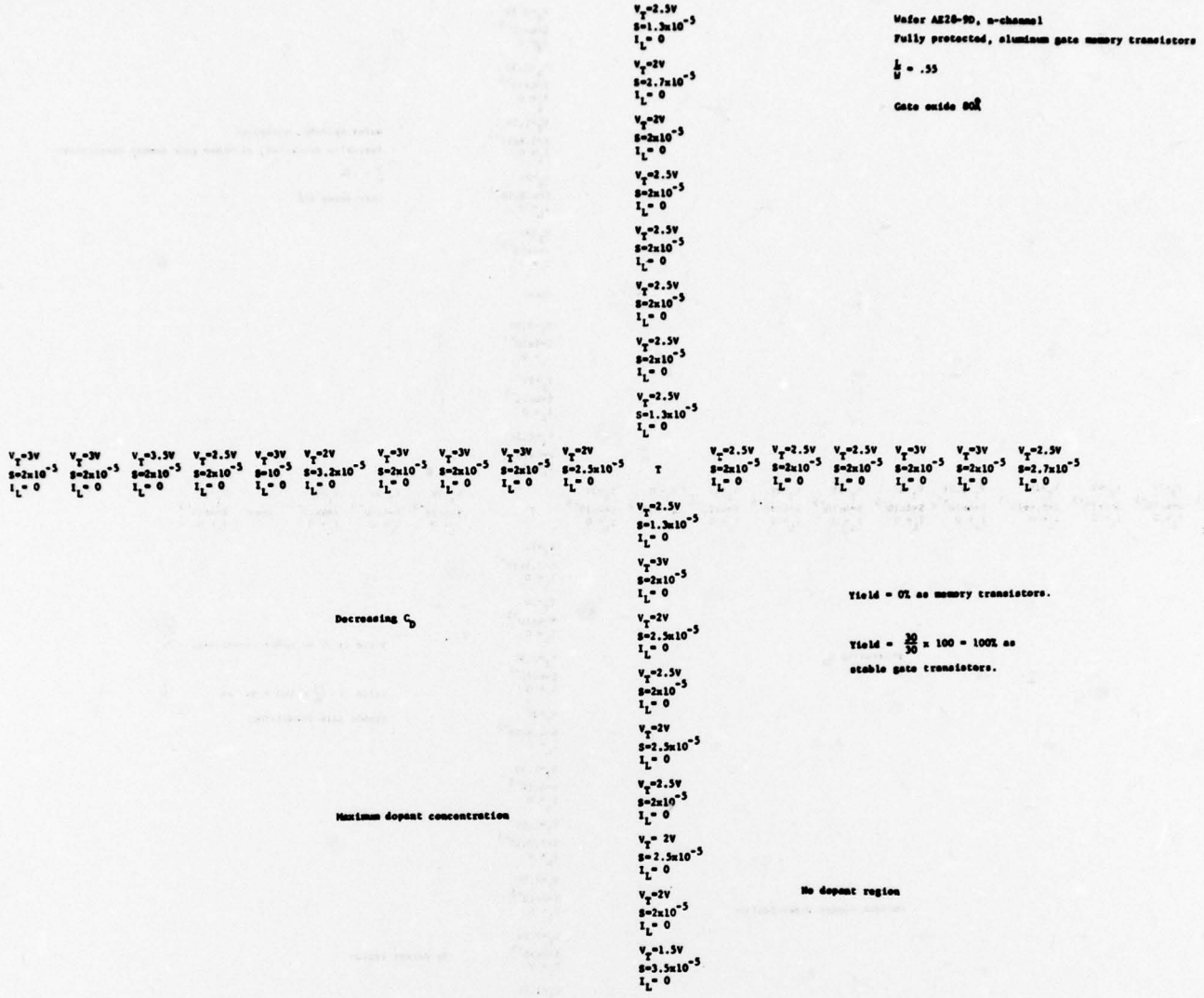


Figure 111B. Yield Survey of Device Characteristics on Wafer A28-9D, Stable Gate and Memory Devices

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

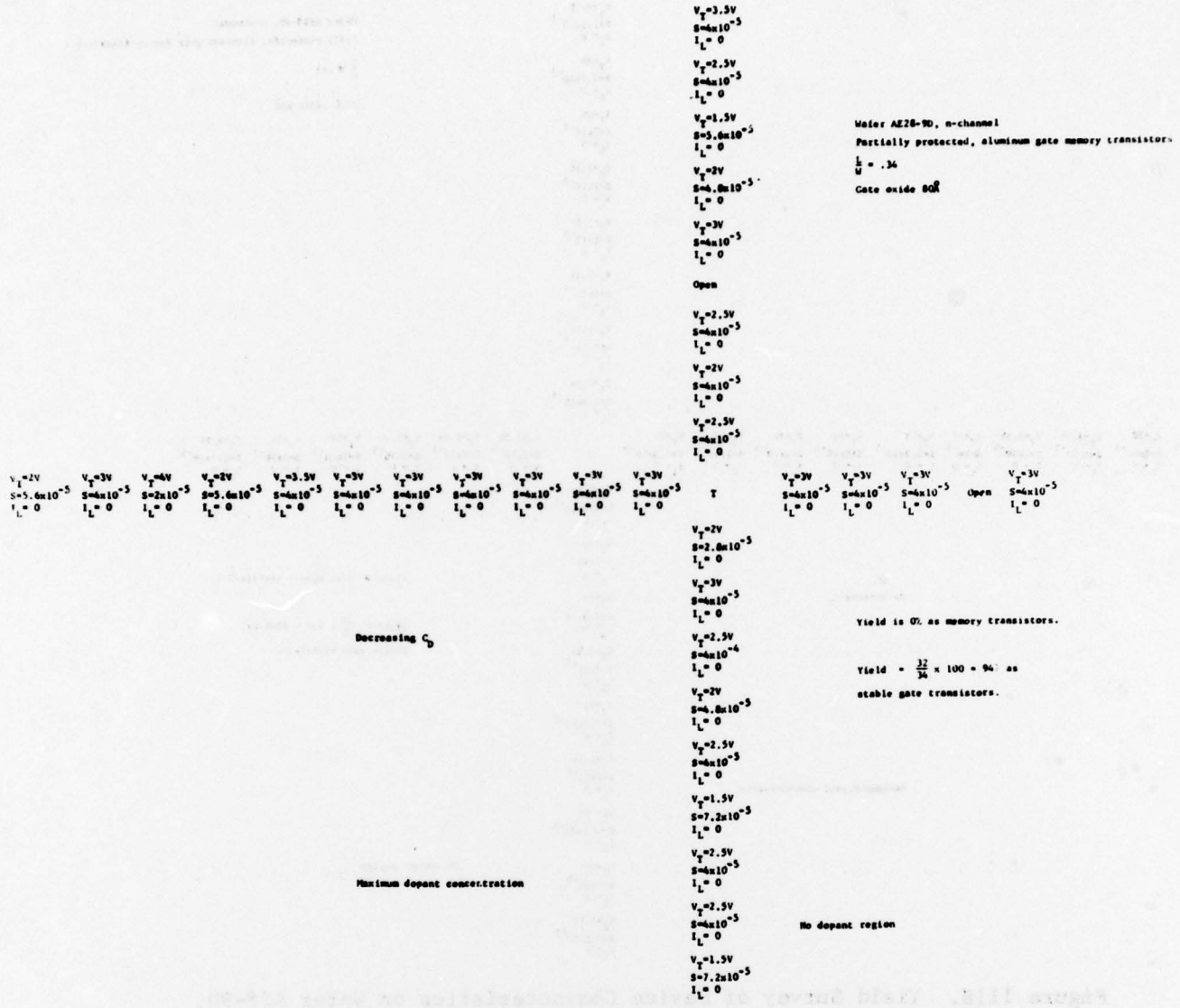


Figure 111C. Yield Survey of Device Characteristics on Wafer A28-9D, Stable Gate and Memory Devices

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

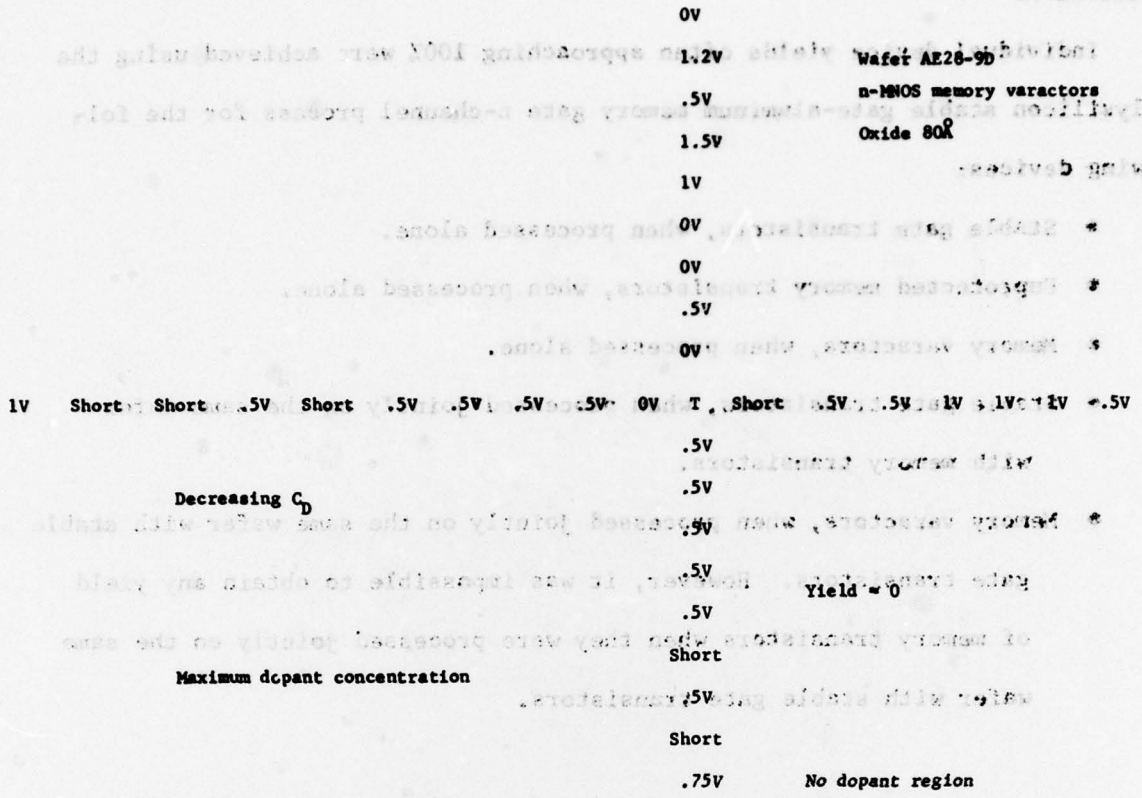


Figure 111D. Yield Survey of Device Characteristics on Wafer A28-9D, Stable Gate and Memory Devices

CONCLUSIONS

Individual device yields often approaching 100% were achieved using the polysilicon stable gate-aluminum memory gate n-channel process for the following devices:

- Stable gate transistors, when processed alone.
- Unprotected memory transistors, when processed alone.
- Memory varactors, when processed alone.
- Stable gate transistors, when processed jointly on the same wafer with memory transistors.
- Memory varactors, when processed jointly on the same wafer with stable gate transistors. However, it was impossible to obtain any yield of memory transistors when they were processed jointly on the same wafer with stable gate transistors.

SECTION XII

CONCLUSIONS

An important figure of merit established for MNOS performance is the retention x endurance product, with dimensions of sec x cycles. It was found for conventional MNOS devices that the retention x endurance product is of the order of 10^{16}. If this criterion is applied to the interface doped devices fabricated in this program, it is found that this product is frequently exceeded by many orders of magnitude. This is shown in Table 17 for the six most promising dopants, which are Cr, Pt, W, Ir, Ni, and Pd. It should be noted, however, that this high retention x endurance product is entirely due to the long retention of these devices, rather than their endurance, which was of the order of 1000 cycles for all devices, as discussed above.

The surprising feature displayed by interface doped MNOS devices is that they can show a very high write speed and long retention at the same time. These "optimum" devices are listed in Table 18, which gives the write speed (30 V intersection) as well as the retention obtained. It should be noted that write speeds well below 1 μs can be obtained. This speed can be traded for a smaller write voltage applied for a longer period.

The principal conclusions are as follows:

(1) The six most promising dopants are: Pt, W, Cr, Ni, Pd, Ir.

(2) The stored charge is principally negative. A one-transistor cell is, therefore, compatible with n-channel circuitry.

(3) Interface doped MNOS devices differ from undoped ones principally in their ability to eject stored negative charge.

(4) Thinner oxide, thinner nitride, and high dopant concentration give a faster device. Write times as short as 2 nsec are possible.

TABLE 17

ENDURANCE X RETENTION PRODUCT FOR

DEVICES WITH THE 6 MOST PROMISING DOPANTS

P-CHANNEL

DOPANT	DOPANT CONC. $\times 10^{15}$ CM^{-2}	d_{ox} Å	d_N Å	ExR CYCLE-SEC
Cr	2.95	134	452	3.29×10^{22}
	"	53	"	1.05×10^{12}
	8.6	53	"	4.8×10^{9}
	"	134	"	8.55×10^{18}
Cr	0.77	61	372	2.4×10^{19}
	"	134	"	5.12×10^{17}
Cr	5.2	43	263	7.7×10^{14}
Cr	1.1	57	263	8.0×10^{23}
Cr	0.81	85	372	8.0×10^{20}
	3.9	"	"	5.4×10^{17}
	3.9	"	"	1.53×10^{19}
Pt	1.12	85	372	7.8×10^{25}
	0.27	"	"	1.2×10^{24}
Pt	0.12	58	320	1.15×10^{15}
W	0.55	63	450	8.0×10^{22}
W	1.08	68	439	3.3×10^{16}
W	2.8	68	"	4.4×10^{24}
W	1.79	84	280	5.06×10^{16}
W	1.94	58	320	6.55×10^{18}
Ir	0.08	53	468	2.2×10^{12}
	"	80	"	2.0×10^{23}
Ir	1.09	80	"	4.2×10^{12}
Ir	0.15	58	320	2.16×10^{17}
Ni	1.22	53	468	1.26×10^{16}
	"	85	"	3.4×10^{13}
	0.27	85	"	1×10^{24}
Pd	0.86	85	372	1.6×10^{25}
	1.58	85	"	7.7×10^{25}

TABLE 17 (Cont'd.)

N-CHANNEL

DOPANT	DOPANT CONC.	d_{ox} Å	d_N Å	ExR CYCLE-SEC
Ir	1.1	80	350	10^{29}
	0.3	80	350	2.4×10^{25}
	0.3	64	350	3.2×10^{17}
Pt	0.8	64	"	4.8×10^{19}
	2.7	85	"	3×10^{11}

TABLE 18

OPTIMUM DEVICES

P-CHANNEL

Dopant	Conc. $\times 10^{15}$ cm^{-2}	d_{ox}	d_N	Window	Write Speed	τ_r sec	t_R sec
Cr	1.1	57A	263A	6.4V	0.4 μs	8.0×10^{10}	4.0×10^{18}
Cr	5.4	50	263	5.4	0.35	1.0×10^{7}	4.6×10^{10}
Pt	0.27	85	372	5.4	2.5	1.7×10^{13}	6.0×10^{19}
Pt	0.27	85	372	9.2	0.25	2.2×10^{14}	1.3×10^{21}
Pt	0.12	58	320	4.4	0.15	3.0×10^{6}	2.4×10^{12}
W	1.94	58	320	7.7	0.002	4.8×10^{8}	7.8×10^{13}
W	1.8	84	280	9.5	0.6	1.7×10^{7}	2.2×10^{12}
Pd	1.58	85	372	4.3	0.065	4.0×10^{13}	1.1×10^{22}
Ni	0.66	58	320	6.1	0.02	5.8×10^{8}	1.2×10^{15}
Cr	1.59	85	372	6.4	3.2	3.5×10^{10}	9.0×10^{15}

N-CHANNEL

Pt	0.8	64	350	9.6	2	6×10^{11}	8×10^{17}
	2.7	85	"	9.2	1	8×10^{4}	2.1×10^{9}
Cr	1.7	64	"	6.1	40	6×10^{12}	4×10^{20}
Ir	0.3	64	"	3.4	80	8×10^{6}	4×10^{15}

(5) Surface state generation occurs at gate voltages of > +20V if applied for more than several seconds, but not for gate voltages < -20V.

(6) Interface doped MNOS devices have much higher retention than undoped MNOS devices of equivalent write speed.

(7) Even the retention of fast write (< 1 μs) devices can be very long (10^5 to 10^{17} s).

(8) Thick oxide, thick nitride, and a low dopant concentration favor higher retention.

(9) Retention is controlled by back-tunneling between 77°K and 300°C.

(10) Write/erase cycling does not affect retention.

(11) The effective endurance of interface doped MNOS devices is 10^3 write/erase cycles.

(12) Write/erase cycling beyond 10^3 cycles is accompanied by the rapid formation of surface states for p-channel devices, but no increase in the surface state density is observed in n-channel devices.

(13) We cannot trade retention for endurance.

(14) Device yields of 80% or better were achievable using the polysilicon stable gate-aluminum memory gate process for the following devices: stable gate transistors, unprotected memory transistors, memory varactors, when processed alone; also stable gate transistors when processed jointly on the same wafer with memory transistors, and memory varactors when processed jointly on the same wafer with stable gate transistors.

(15) Memory transistors could not be processed jointly on the same wafer with stable gate transistors.

(16) The hardness toward total dose ionizing radiation of stable gate interface doped MNOS p- or n-channel transistors is 10^5 rads (Si) for 0 or

-10V gate bias, and 10^3 to 10^4 rads (Si) for + 10V gate bias. Cr doping increases the hardness 10X.

(17) Memory transistors, when exposed to ionizing radiation, experience window closure at 10^6 rads, at zero gate bias. They can be fully re-written after exposure.

APPENDIX

CORRELATION OF ELECTRON BEAM AND Co^{60} RADIATION RESULTS

Close agreement was observed between the effects of high energy electron beam and Co^{60} gamma irradiation of both stable gate and memory transistors. To obtain evidence supporting this empirical observation, CaF_2:Mn thermoluminescent dosimeters (TLD), obtained from the Harshaw Chemical Company, were used to calibrate the 1.5 MeV electron beam source. Similar dosimeters were then irradiated during the course of the Co^{60} device testing at CRL. Results of the two were then compared.

CALIBRATION OF ELECTRON ACCELERATOR

Prior to the preliminary device testing in the on-site electron accelerator facility, over ten TLD's were exposed for varying lengths of time at a number of distances from an on-site Co^{60} source whose initial activity was measured at 15 mC. Given an exposure time and a distance from a Co^{60} source of known strength, the dose received by the dosimeter can be accurately computed and related in units of rads (Si). The known doses received by the TLD's were then directly related to the crystal lattice damage suffered during exposure.

Crystal lattice damage is proportional to the amount of energy absorbed by the sample (via electron ejection and entrapment). To measure this energy, the crystals were heated in the Harshaw 2000A Thermoluminescence Detector. The light given off was monitored by a photomultiplier and the current it produced was integrated to yield charge. It is this measured charge which is directly related to the dose. A given charge implies a certain dose in rads (Si).

These TLD's were then annealed and exposed to the electron gun emissions. The charge "acquired" was measured and translated into rads (Si). In Fig. 1 , the charge measured is plotted as a function of dose for the electron accelerator (the curve marked "Electron Beam").

CRL Co^{60} SOURCE

Thermoluminescent crystals identical to the ones used earlier were included in a number of exposures during the course of the transistor testing at CRL. From measurements of their thermoluminescence made after exposure, the second curve (labeled Co^{60}) was made. Notice that, despite the disparate strengths of the calibration Co^{60} source and the CRL Co^{60} source, the curves agree to within a factor of three.

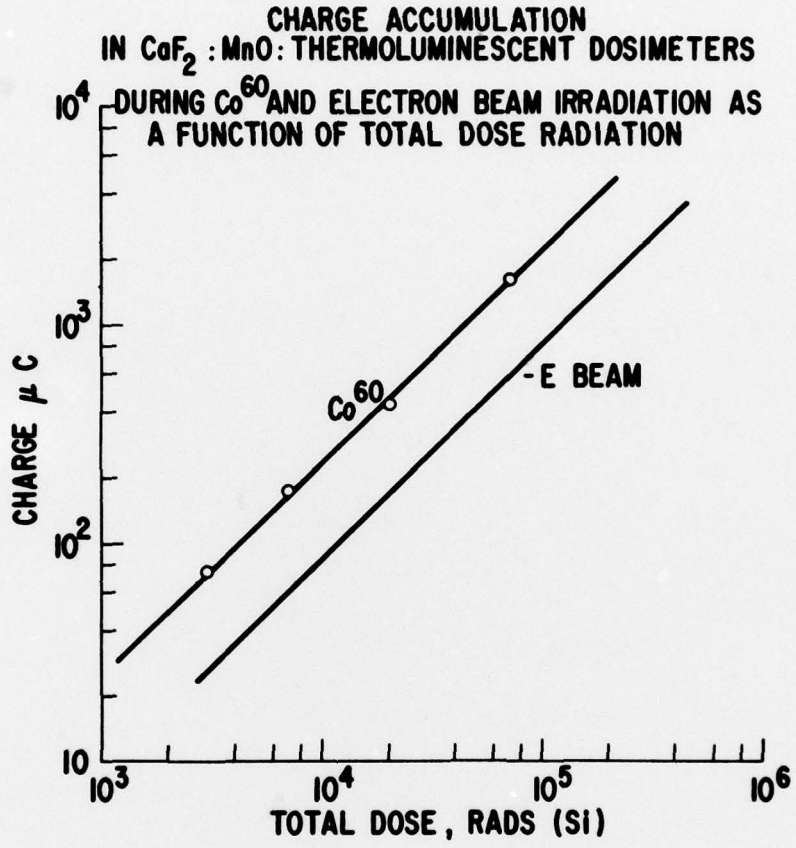


Figure 112. Charge Accumulation in CaF_2:MnO Thermoluminescent Dosimeters During Co^{60} and Electron Beam Irradiation as a Function of Total Dose Radiation

*U.S.Government Printing Office: 1979 — 657-002/518